Power Electronics

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July 13, 2010

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Preface and introduction

Preface and acknowledgements

This text comes from my lecture notes, taken during the course of Power Electronics, held by Professor Franco Maddaleno during the academic year 2009/2010 at Politecnico di Torino.

I am writing this preface for some reasons: first of all I want to thank all my colleagues and friends which supported me writing all this stuff, helping me finding and correcting mistakes, or improving my work; I want to thank Francesco Laviola, Salvatore Galfano, Elena Ruo Rui and Vittorio Gilli, who gave me indications about some mistakes; very very very special thanks especially for Marco Elia, which gave me a **huge** help with all my mistakes: thank you guys!

Something else: even if this is not the first text I have written in english, every time I read it I see some mistakes, often caused by haste, and I have no time to correct them (so sometimes I have to upgrade this text), given many problems to my mates; first reason so is my desire to apologize with the students that will read these notes, hoping that, despite of my poor english, they will appreciate them.

One last note: unlike other text written by me, for this one I decided to spend some more time, to introduce images and schematics; I spent a lot of time searching for some methods or programs aimed to draw in LaTeX, and I have to thank again Francesco Laviola, for an advice he gave me: "latexdraw". This program has a GUI in which we can draw something, and obtain instantly the PSTricks code, which can be integrated in the TeXdocument. For electronic circuits, I prepared some templates for this software, templates which will be eventually available in some site (when I will have time to organize and upload them!), in a sunny Saturday afternoon (so now **you** have to thank **me**! :-P).

Latexdraw is available at the following address:

`http://latexdraw.sourceforge.net/`

Use it! It is awesome!

About other drawings, like mathematical plots, my idea is to use a **tikz** application, which joins LaTeXand **gnuplot**, but it is in a *testing phase* (about me: no time to use it :-( ). We will see, next time.

So, now, I wish you all a good read.

Alberto Tibaldi

Introduction to power electronics

When we talk about electronics, we can find at least two branches: signal electronics, and power electronics. In this text we are interested to talk about power electronics, and power electronics is **efficiency**: every time we worry about efficiency we are talking about power. With power electronics we can consider power in the order of magnitude of watts, kilowatts, megawatts, but this does not care: this text will predominantly be focused on efficiency. Of all the possible operations, the main one, in this course, will be the DC to DC conversion (and some AC to DC).

Why is efficiency so important? Well, let's consider for example a cell phone: we want to maximize the time of a battery, and this is a problem of efficiency, so of power electronics: we are not interested in power level, but in the duration of the battery, and it depends on the efficiency of the DC-DC conversion hidden inside the cell phone.

We are going to study power levels up to 1 kilowatt, but this is not important: the important thing is to acquire some concepts.

Efficiency is usually expressed with η:

$$\eta \triangleq \frac{P_{\text{out}}}{P_{\text{in}}} \leq 1$$

Let's remark that η is **always** less or equal (but, in real world, all the times less) then 1: we can not have, out of a system, more power then the input one!

Efficiency is an important parameter: we have to increase it, for a number of reasons; let's find them! We can see that:

$$P_{\text{out}} = \eta P_{\text{in}} \Longrightarrow P_{\text{in}} - P_{\text{out}} = \text{dissipated power (heat)} \triangleq P_{\text{diss}}$$

So:

$$P_{\text{diss}} = P_{\text{in}}\,(1-\eta)$$

In other words:

$$P_{\text{out}} \frac{1-\eta}{\eta} = P_{\text{diss}}$$

This is very important because, if we have high efficiency, we have advantages! In fact, if η decreases, we have higher costs (because we need more input power); if we have a limited power source, like a battery, we **need** high efficiency, if we want that battery lasts longer!

From the last equation, if we have $\eta \sim 1$, we have a very small numerator; this reduces dissipated power, so heat! High temperature is bad because it

can damage circuits, and we want to ensure the reliability of the circuit. A standard rule is: if we increase the temperature, the lifetime of the system decreases as a power of 2: with 10 °C we make lifetime decrease by a factor of 2, 40 °C makes lifetime decrease of $2^4 = 16$ times. This means that we have to design better cooling systems, so heavier and/or larger objects, or more fans.

Let's consider this numerical example: if we want an output power of 100 W, with $\eta = 90\%$, we have:

$$P_{\text{in}} = \frac{100 \text{ W}}{0.9} = 111 \text{ W}$$

So:

$$P_{\text{diss}} = (111 - 100) \text{ W} = 11 \text{ W}$$

So, we have to remove 11 W. If efficiency is 80%, we have:

$$P_{\text{in}} = \frac{100 \text{ W}}{0.8} = 125 \text{ W}$$

So, we have 25 W of dissipated power; that's a lot! More then the double! We need a larger box, a heavier heatsink!

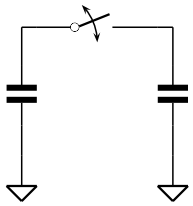
Components

Which components can we use, in power electronics? Well, we already said that the main goal is to increase efficiency, so reduce losses; we need to avoid components which dissipate too much power.

Capacitor and inductor are obviously good components: they are **reactive** components, so, ideally, they don't dissipate any energy. Diodes are a little worse: they have a voltage drop on them (about 1 V, for power diodes), but they can be used. What about transistors? Well, it depends: if we use a transistor in linear zone or as a switch, from the power point of view it changes everything! As switch it is ok, but in linear zone absolutely not! And resistors? Well, their main job is to dissipate, power, so, for our purpose, we can not use them! In power stage we will **not** introduce resistors (but in the control stage, obviously, there are no problems!)

We will mainly use, in the power stages, capacitors, inductors, diodes, switches (realized with transistors in saturation or interdiction zones).

Now, a question: can we use, to realize our power stage, just switches and capacitors?



The answer is **no**: if we have two capacitors and a switch, supposing that one has on it a voltage $V(0)$ before closing the switch, and so a charge equal to:

$$Q(0) = CV(0)$$

Where C is the value of the capacitance (and 0 is the time when we evaluate voltage and charge). The other one is empty. After the transient, in steady state, supposing that the two capacitances are equal, we have:

$$V_1(\infty) = V_2(\infty) = \frac{V(0)}{2}$$

This means that voltage of the left capacitor is halved. What about energy? Well, we have that, in the left capacitor, we have:

$$E(0) = \frac{1}{2}CV(0)^2$$

The final energy will be:

$$E(\infty) = \frac{1}{2}C\left(\frac{V(0)}{2}\right)^2 = \frac{1}{8}CV(0)^2$$

This, for each capacitor; the total final energy will be the double of this:

$$E_{\text{tot}} = \frac{1}{4}CV(0)^2$$

so, half of the former energy. We have lost somewhere energy, even if the switch is ideal (there are many interpretations: or irradiation, or small leakage through parasite resistances which model a small non-ideality).

The only ways to charge a capacitor without any loss is via a current source (so something which can maintain constant the current on it), or an **inductor**.

Let's remember that the differential equation which describes an inductor is:

$$V_L = L\frac{\mathrm{d}i_L}{\mathrm{d}t}$$

Let's consider a simple example of solution of this differential equation, which will be used soon: if we want constant voltage V_L, we need i_L to be a ramp, a line. In this case, we have that:

$$\frac{\mathrm{d}i_L}{\mathrm{d}t} = \text{constant}$$

So, slope will be equal to:

$$\frac{\mathrm{d}i_L}{\mathrm{d}t} = \frac{V_L}{L}$$

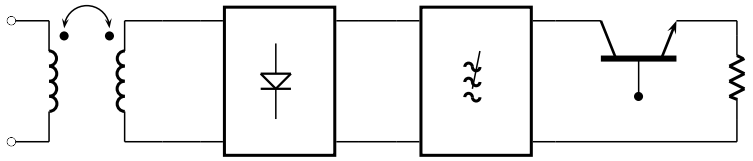
This is the differential equation we will mainly use in this text.

Chapter 1

Switch-mode power supplies

1.1 Introduction

We want to compare these supplies with linear power supplies. Their basic schematic is:



It has a 50 Hz transformer, some diode bridge to rectify the signal, and a big capacitor in parallel of the output; most of the times there is a transistor which controls the system.

Let's see the advantages of switch-mode power supplies respect to these ones:

- the first advantage is efficiency: switch-mode supplies have an efficiency from 70% to 95% ;
- the linear regulator has an output voltage which is all the times less then the input one: there is **always** a voltage drop, which permits to maintain constant the output voltage value; switch-mode supplies has no limitations of V_{out} versus V_{in}: we can obtain $V_{\text{out}} > V_{\text{in}}$, and also opposite polarities;
- we can obtain isolation with switch-mode supplies in a better and simpler way, because we don't have any 50 Hz transformer, but high frequency transformer (smaller and cheaper);

- we can have multiple outputs;
- circuit is smaller, for two reasons: first, because high efficiency requires less coolers; high frequency generally is associated with smaller components, so the whole circuit will be smaller, and will cost less.

Switch-mode power supplies have also some drawbacks:

- they are complicated: we need at least two university courses to learn them;
- they are very noisy;
- they are slower (they have a smaller bandwidth): if the load changes, their output voltage changes slower respect to linear power supplies one.

1.1.1 Introduction to basic topologies of switching-mode converters

In this subsection we will only show slowly the main properties of the basic switching topologies for converters; in the following sections, we will study in details every one of them.

The two basic topologies are:

- **buck**: we have $V_0 < V_{\text{in}}$;
- **boost**: we have $V_0 > V_{\text{in}}$.

This is not true: it assumes to be **positive voltages**, so *in modulus* they are true.

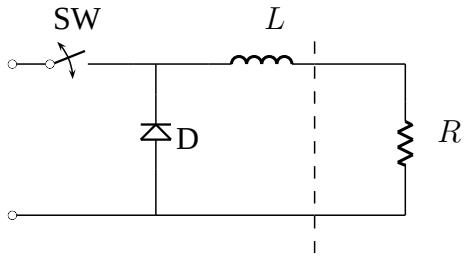
Buck and boost topologies are dual, and they are the basic topologies; this means that every other topology derives from them. There are at least two other main topologies (not basic, because derived from the previous ones):

- **buck-boost**: it is a very old circuit (formerly known as **flyback**); someone analyzed this topology, and discovered that it is just a combination of the first ones; it provides $V_{\text{in}}V_0 < 0$, but exists also a non-opposite polarity version.
- **boost-buck** (mainly known as Čuk converter): the opposite.

Now, as already written, we will analyze quite in depth these four topologies.

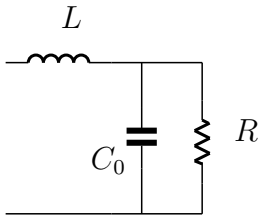
1.2 Buck converters

If we look a power electronics book, we can see that, theoretically, a buck converter is something like this:



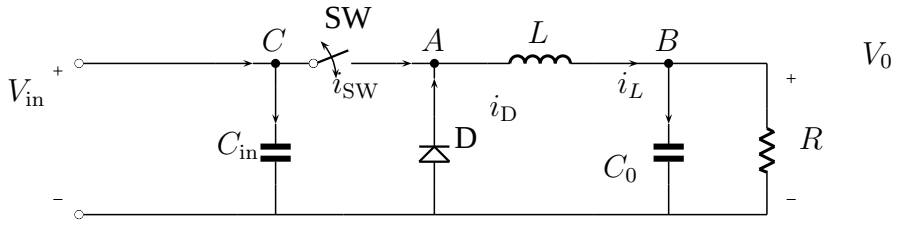
This is **NOT** the schematic of an actual buck converter: there are two more components, which are **mandatory** if we want a working converter.

Let's observe that L and R (where R is the load of our circuit) in series form a filter (a low-pass filter); this is not the best we can do: we can use a second order filter instead of a first order one, so introduce an output capacitor, C_0. This is the output stage of the buck converter.



We have also and especially to introduce an input capacitor, also if we are using a DC voltage supply: ideal supplies **do not exist**, because, in real world, we have just **real** voltage sources! We need to introduce **absolutely** an input capacitor C_i, which is also the first tool that can remove electromagnetic emissions.

The final schematic of a **real** buck converter is this:



In order to do the analysis, we are going to introduce four assumptions, four hypothesis:

- low losses (so, to have **ideal** components): we will remove later this assumption; we consider ideal diode (so, voltage drop equal to zero), ideal inductors, capacitors (without parasites), and switches;
- we consider to have time constants very higher respect to the switching period T_{switch} (which will generally be called simply T_{SW});
- we consider **constant** the output voltage, so we don't consider ripples; in lab we can see the ripples, but now we are not going to introduce it, in our analysis;
- just for the first analysis, we assume to have a **cyclostationary** state: it is not exactly a steady state, because we don't have a DC bias point, but something similar: now, we are ignoring transients.

Another thing: we are assuming that switching frequency is **constant**: this is an hypothesis we will use for most of our circuits (we will talk about switching frequency later).

We have to distinguish two different working modes:

- CCM: i_L must be different from zero for every time; this is called **Continuous Conduction Mode**;
- DCM: there exists a time interval t when $i_L = 0$; this is called **Discontinuous Conduction Mode**.

Let's analyze this circuit: we are considering a condition similar to steady state (cyclostationary), so we have:

$$\overline{v_L} = \left\langle L \frac{\mathrm{d}i_L}{\mathrm{d}t} \right\rangle$$

but L is a constant, and derivative is a linear operation, so we can do the average of just i_{L}:

$$= L \frac{\mathrm{d}\langle i_L \rangle}{\mathrm{d}t} = 0$$

but so we are differentiating an average, and an average is a number, so we obtain zero! Using the same ideas, we can find that

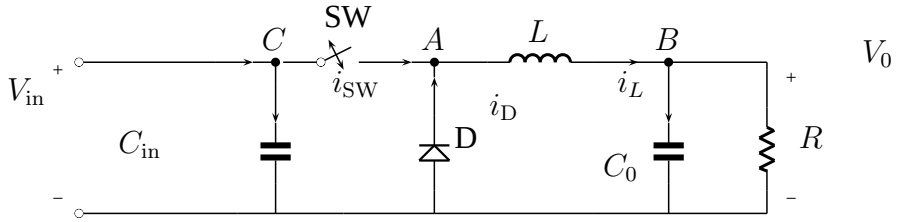
$$\overline{i_C} = 0$$

A remark: there is just a situation where a capacitor has voltage on it with non-zero DC: if it is **broken**!

As first step, we want to analyze the current on the inductor, i_L, versus the time t:

$$i_L = \frac{1}{L}\int_0^t v_L(\tau)\mathrm{d}\tau + i_L(0)$$

This is a definition which obviously works, but that it is also hard to study: this is for mathematicians! Let's think like engineers: we assumed that we have always constant voltages, so, like previously said, with constant voltage on the inductor we have a current with ramp behaviour! It can be an up-ramping, or a down-ramping. Let's consider this convention:



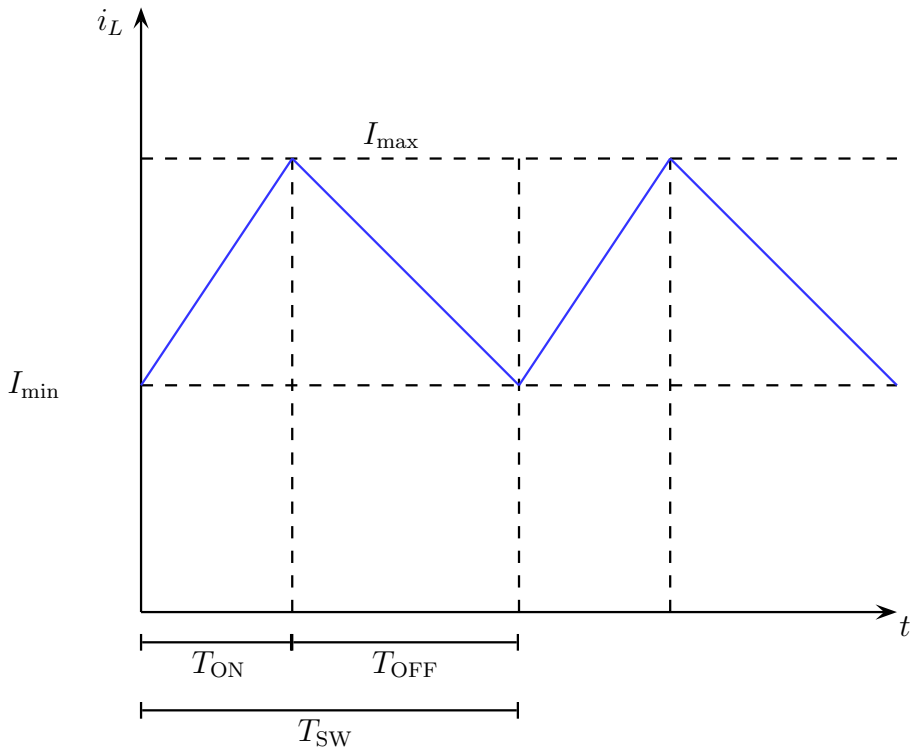
The slope of the ramp will be

$$\frac{\mathrm{d}\langle i_L\rangle}{\mathrm{d}t} = \frac{V_L}{L}$$

If we have non-ideal inductors, we have an exponential behaviour instead of a ramp behaviour; this is not so important, because we consider short time intervals, so we basically see a linear behaviour.

1.2.1 CCM analysis

In CCM, we have that current is never zero; this means that we will have a $I_{\max}$ value, and a $I_{\min}$ value, both non-zero (and, for hypothesis, higher than 0):



The initial value of the current through the inductor is not zero: we start with an initial $I_{\min}$, and, for hypothesis, with the switch **closed**; we call the time when the switch is closed T_{ON}, and the one with the switch open T_{OFF}; obviously, we have that:

$$T_{\text{SW}} = T_{\text{ON}} + T_{\text{OFF}}$$

where T_{SW} is the switching period (T_{switch}).

We are studying a buck converter, so we have an output voltage less than the input one; considering the previously showed convention, we have that, during T_{ON}:

$$V_{\text{L}} = V_{\text{in}} - V_0$$

because the switch connects directly the input voltage source to the left pin of the inductor, and the right one is always connected to the load, so to the output. This means that the slope of the current is:

$$\frac{\mathrm{d}i_L}{\mathrm{d}t} = \frac{V_{\text{in}} - V_0}{L}$$

After T_{ON} we obtain a current value equal to $I_{\max}$.

When the switch is open, the current through the inductance is continuous: the current through an inductance in fact is a state variable, because:

$$E_L = \frac{1}{2} L i_L^2$$

We can't have energy steps, so also current steps! Another way to say it is that the state variable keeps the memory of the previous states of the device, because the device can keep energy! Talk about poles, energy, memory, is the same thing.

Current so keeps flowing through the inductor: we can't stop it (without having huge voltage increases); the diode permits current to flow: this diode is called **free-wheeling**. The diode is so mandatory, and must be mounted in the correct way: if we forget it, the current on the inductance changes quickly, so the voltage on the inductance increases, the switch goes in avalanche, and probably the circuit get damaged. The diode behaves ideally as a short circuit. During this time interval, T_{OFF}, we have zero-voltage at the left pin (in fact, we are ignoring the voltage drop on the diode), obtaining:

$$\frac{\mathrm{d}i_L}{\mathrm{d}t} = -\frac{V_0}{L}$$

After T_{OFF}, so once ended a cycle T_{SW}, we obtain again I_{min}; is it strange? No! We are assuming to be in a cyclostationary state, so it is absolutely normal!

If we impose the cyclostationary condition, we can say that:

$$\frac{V_{\mathrm{in}} - V_0}{L} T_{\mathrm{ON}} + \frac{-V_0}{L} T_{\mathrm{OFF}} = 0$$

this, because, after a cycle, the current does not change at all! At the end of a cycle, we have the same current! So:

$$V_{\mathrm{in}} T_{\mathrm{ON}} - V_0 \left(T_{\mathrm{ON}} + T_{\mathrm{OFF}}\right) = 0$$

so

$$V_{\mathrm{in}} T_{\mathrm{ON}} = V_0 T_{\mathrm{SW}}$$

So:

$$\frac{V_0}{V_{\mathrm{in}}} = \frac{T_{\mathrm{ON}}}{T_{\mathrm{SW}}}$$

The ratio of the ON time respect to the full switching time is called **duty cycle**, D (or **duty ratio**):

$$D \triangleq \frac{T_{\mathrm{ON}}}{T_{\mathrm{SW}}}$$

The ratio of V_0 over V_{in} is called M:

$$M \triangleq \frac{V_0}{V_{\mathrm{in}}}$$

In the buck converter case, we have:

$$M = D$$

This is, obviously, a particular case.

Now, a question: why are we using an inductor L? Can't we avoid it? Well, we need it, because, if $L = 0$, we are dividing by zero an expression; this can be said also with circuital observations, but the main reason is this one.

If we remove the low-losses hypothesis, we have:

$$T_{\mathrm{ON}} \frac{V_{\mathrm{in}} - V_{\mathrm{SW}} - V_0}{L} + \frac{-V_{\mathrm{D}} - V_0}{L} T_{\mathrm{OFF}} = 0$$

Where V_{SW} is the voltage drop on the switch, and V_{D} the voltage drop on the diode; the resulting expression is a function of the duty cycle D, of the input voltage, and of the voltage drops on diode and switch. It is good that D stills controls the output: we can control it, so also the output! Same thing for V_{in}. What we can do is solve this equation, and, once designed the value of D, increase it a little, in order to compensate the voltage drops.

Parameters

There are three parameters which can quantify the quality of the converters:

$$\left.\frac{\partial V_0}{\partial V_{\mathrm{in}}}\right|_{D=\mathrm{constant}} = \text{Audio susceptibility}$$

Its name derives from the theory of the old audio amplifiers.

$$\frac{\partial V_0}{\partial D} = \text{Gain}$$

This is the gain.

$$\frac{\partial V_0}{\partial I_0} = \text{Output resistance}$$

We are deriving a voltage respect to a current: this is, dimensionally, a resistance: the output resistance.

There is another version of these parameters, useful for lab measurements:

$$\frac{\Delta V_0}{\Delta V_{\text{in}}} = \text{Line regulation}$$

$$\frac{\Delta V_0}{\Delta D} = \text{(no name)}$$

$$\frac{\Delta V_0}{\Delta I_0} = \text{Load regulation}$$

They are not easy to calculate.

Let's characterize the buck converter respect to the first three parameters:

$$\left.\frac{\partial V_0}{\partial V_{\text{in}}}\right|_{D=\text{constant}} = D = M$$

This is a result that we will find all the times: the audio susceptibility is always equal to M, and, this time, also to D.

$$\frac{\partial V_0}{\partial D} = V_{\text{in}}$$

This is strange: we have a gain measured in volts, and which can be variable: this is intuitive, because, if we change input voltage, we have to be the same output voltage, so, obviously, gain changes! Ending:

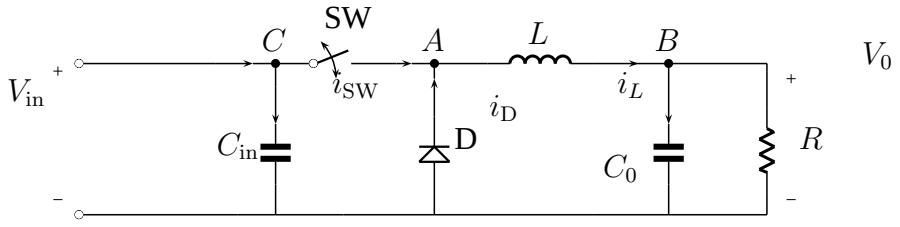
$$\frac{\partial V_0}{\partial I_0} = 0$$

In fact, the output voltage V_0 is not function of the output current I_0.

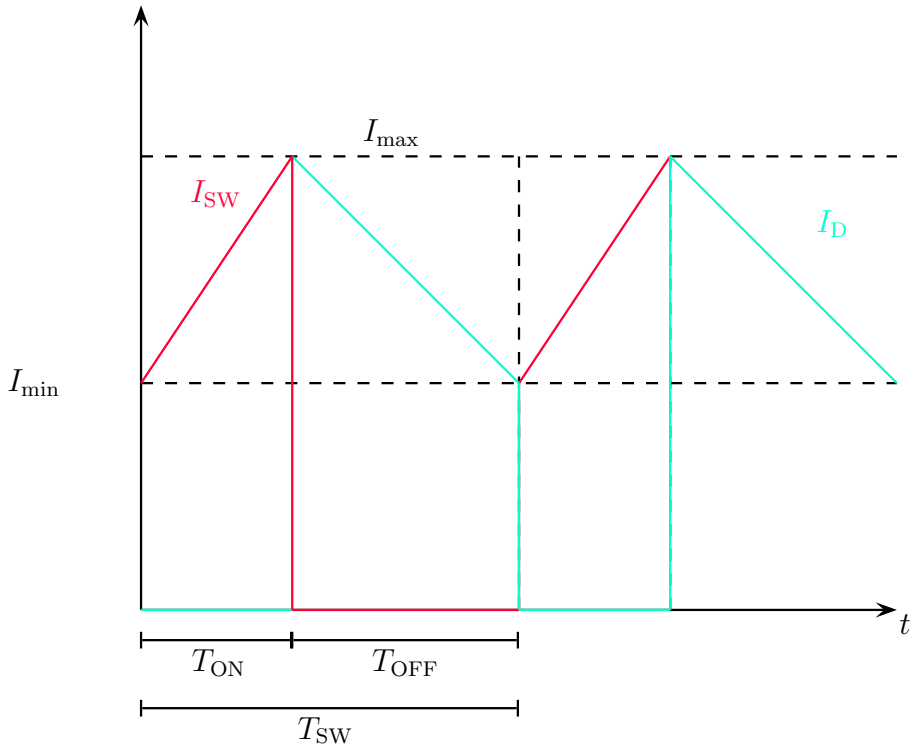
A remark: this topology is one of the most versatile ones! It can work at kilowatts, or megawatts! It is in the cell phones and in personal calculator power supplies, so it is very very versatile!

1.2.2 Circuital analysis

Let's consider this circuit, and all of its quantities (currents and voltages):



The current on the inductor, i_L, as already written, has this graph:



What is I_0 ? Well, we know that, in the output node, we can use KCL (Kirchhoff Current Law), which says that:

$$\sum_{n \in \text{all branches}} i_n = 0$$

Currents are functions of time; what we can do is average both members: the right term is the average of 0, which is 0; for the left member, we remember that average is a linear operator, so that:

$$\overline{\sum_n i_n} = \sum_n \overline{i_n}$$

Now: what is the average of one cycle? Simply, the DC component! In other words, the average of a variable signal is its Fourier transform, evaluated in 0 Hz! In the hypothesis, we said that V_0 has no ripple, so:

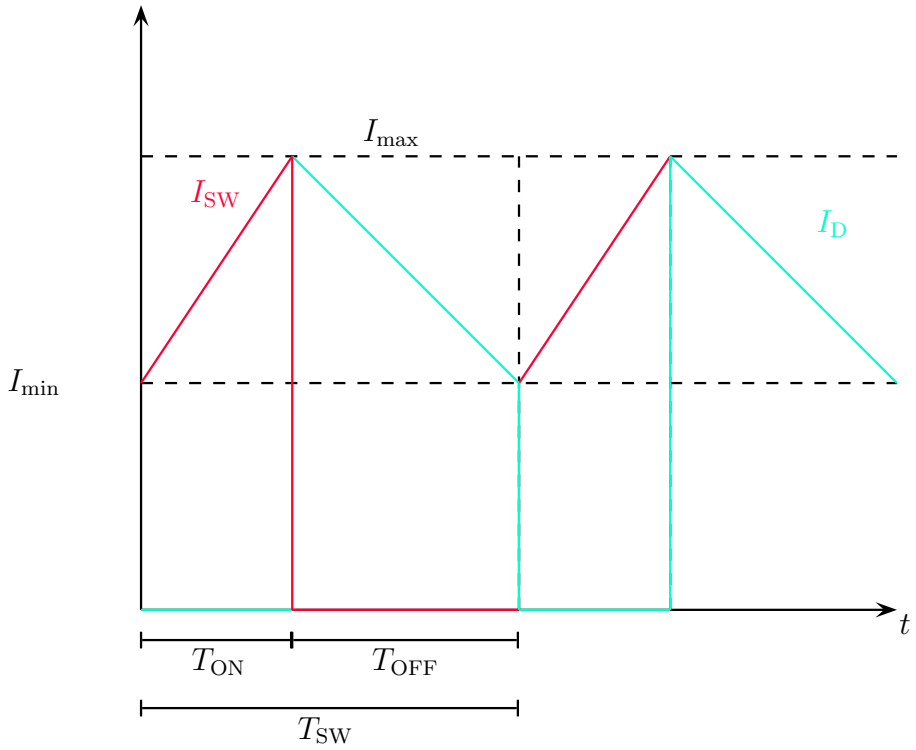
$$I_0 = \frac{V_0}{R}$$

I_0, so, is a DC, because output voltage is constant! We know that, through the capacitor (if it is not broken), DC is zero, so:

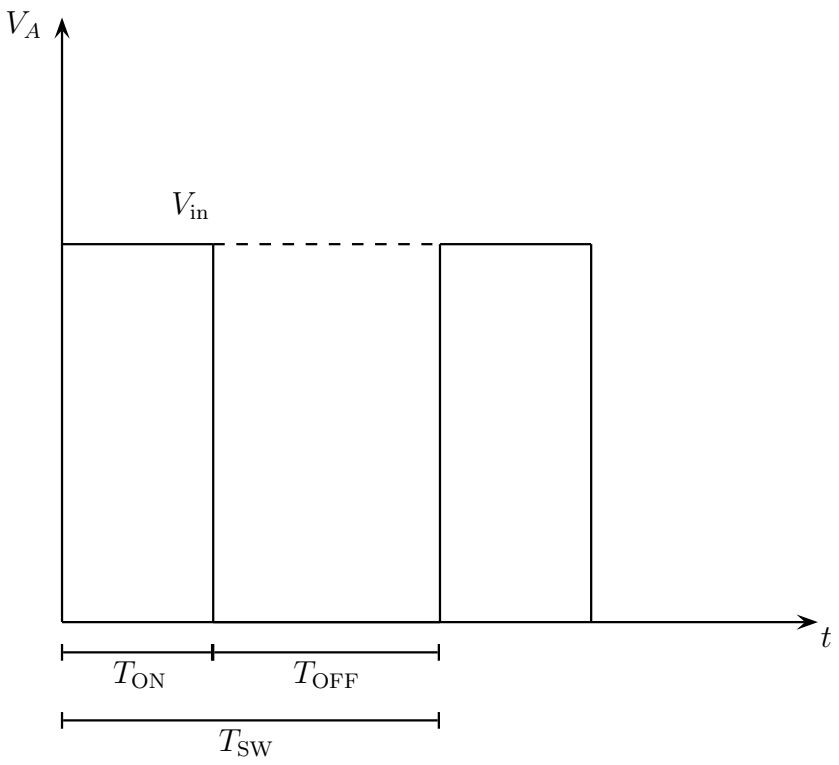
$$\overline{i_L} = I_0$$

In other words, I_0 is equal to the average value of the current through the inductor.

Now, let's consider the currents on the switch and on the diode: I_{SW} is the current on the switch, and we know that, ideally, on the switch there is current only when it is closed; when it is closed, all the inductor's current goes in the switch, so we have, for the T_{ON} interval, that $I_{\text{SW}} = i_L$; in this period, I_{D}, so the current inside the diode, is zero. During T_{OFF}, we have the dual condition: on the switch there is no current, and so all i_L goes into the diode. We have a graph like this one:



We have three more variables to consider; the first one is the voltage on the node A:

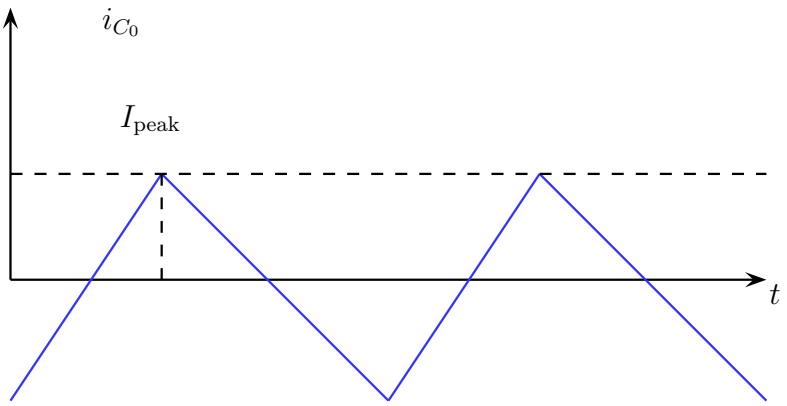


During T_{ON}, we have that the voltage on A is equal to V_{in}; this means that, on the ideal diode, we have a breakdown voltage equal to V_{in}. During T_{OFF}, we consider negligible the voltage drop on the diode, and obtain $V_A = 0$ V.

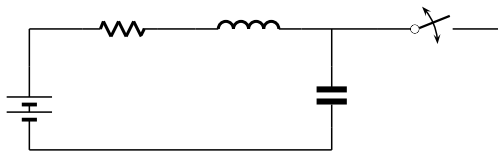
Still two variables: the currents into the two capacitors. About the current on C_0, applying KCL on the output node, we have that:

$$i_{\text{C}_0} = i_L - I_0$$

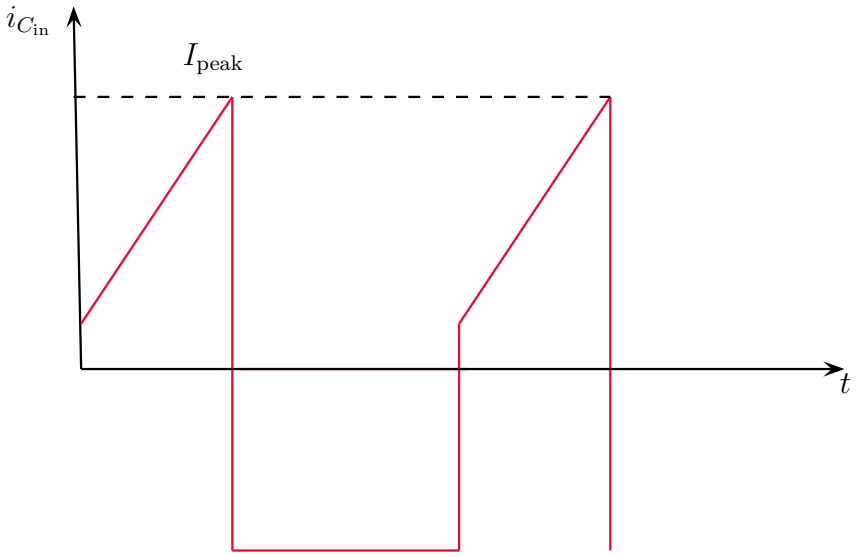
in fact, we have just the ripple current, into the output capacitor!



About the current on the input capacitor, we have to introduce some more assumptions: let's consider the following DC source line:



If we have this circuit, for high frequency components, there are two paths: the inductance and C_i: we suppose that all the current goes into the input capacitor, because the inductance must work as a filter. Obviously, a capacitor can not have a DC component, so we have the current into the switch, without its DC component:



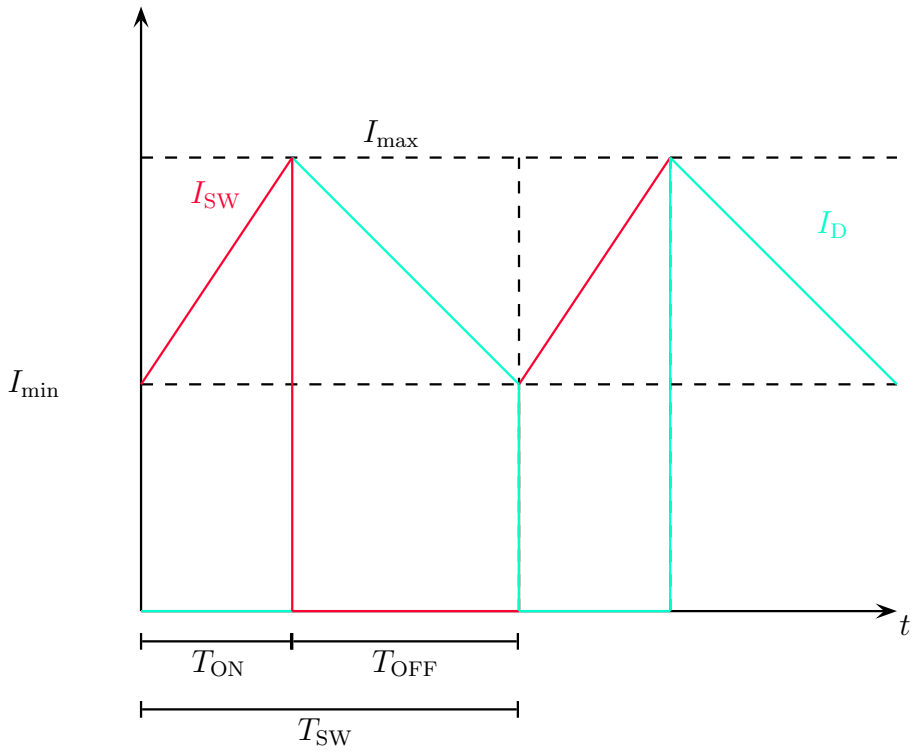
The upper and lower areas must be equal, because the average must be zero.

We have the graphs, but now we need to put numbers in them, in order to understand how much the components are stressed. Let's see: when the switch is closed, the diode has a reverse voltage exactly equal to V_in. What we need is to work with RMS (Root Mean Square) currents: this is important because RMS is strictly connected to ohmic dissipations: if we have dissipations, we have RMS currents, and *viceversa*. We can study the critical components from the RMS currents point of view, in order to understand how much are they stressed (capacitors, inductors, transistors, which have parasite parameters, so ohmic losses).

In this subsection we want to learn some tricks, in order to calculate quickly the RMS value of some expression. There are known expressions, like the triangular one (which is important for our analysis):

$$I_{\text{RMS, triangle}} = \frac{I_{\text{peak,triangle}}}{\sqrt{3}}$$

The problem is that we have more exotic wave shapes, like this one:

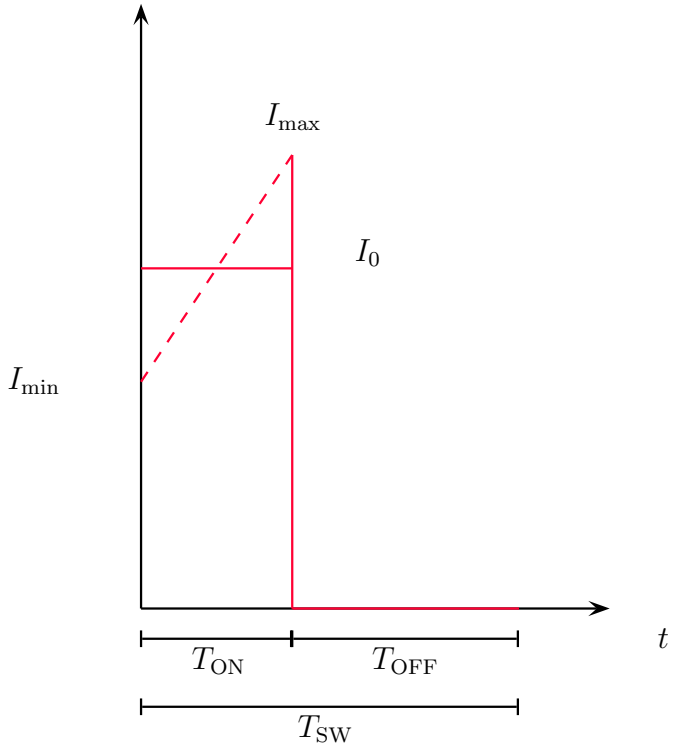


Now, when we have to calculate the RMS value of this wave, we have at least three choices:

- use the RMS definition: RMS means Root Mean Square, so: first operation is the **square** one: we take the signal and square it; then, we **mean** it, so we calculate its average, with its integral; then, **root**: we calculate the square root of the average integral.
- read on a textbook (or in Internet) the formula, which is very complicated:

$$I_{\text{RMS}} = \sqrt{D\frac{I_{\min}^2 + I_{\min}I_{\max} + I_{\max}^2}{3}}$$

- consider, instead of this trapezoidal waveform, an approximated one: I can flat the top, using the average of its value:



Now:

$$I_{\text{RMS}} = I_{\text{flat}}\sqrt{D}$$

where

$$I_{\text{flat}} = \frac{I_{\max} + I_{\min}}{2}$$

(this can be calculated by using the integral of the square waveform, which is very simple).

Now, let's apply it on our cases: we already know I_{flat}, because:

$$I_{\text{flat}} = I_0$$

This can be used in both $I_{\text{SW,RMS}}$ and $I_{\text{D,RMS}}$: in fact, remembering that we have current on the switch during the *positive duty cycle*, the time when the switch is closed (which is associated to the D of the circuit), we have:

$$I_{\mathrm{SW,RMS}} = I_0\sqrt{D}$$

$$I_{\mathrm{D,RMS}} = I_0\sqrt{1-D}$$

Now, let's calculate the RMS current on the output capacitor, C_0: if we use the traditional way, we have to square the triangular function (obtaining parabolas), integrating, and rooting.

We can use the result which says (basing on the Archimede's theorem) that:

$$I^2_{\mathrm{C_0,RMS}} = \frac{\text{Base} \times \text{Height}}{3}$$

Now: base is 1 cycle, so 1 (in other words, $D + (1 - D) = 1$); height is I^2_{pk}, we obtain:

$$I_{\mathrm{C_0,RMS}} = \frac{I_{\mathrm{pk}}}{\sqrt{3}}$$

Now, we have to calculate the last value: the RMS value of i_L. What can we do? Well, the first idea is: may I use KCL on RMS values? No! Absolutely no! RMS values are related to a square of a quantity, and, even if we do the square root, we have just positive values! This says us that:

$$\sum_n i_{\mathrm{RMS}} \neq 0$$

This can be explained in another way: those currents are in fact correlated: given a and b two currents:

$$(a+b)^2 = a^2 + b^2 + 2ab$$

The cross-term is a correlation term. There is just one condition which guarantees that we can use KCL on RMS values: if the terms are uncorrelated.

How can we use this observation? Well, we can see that i_L is a current which has a DC component and an AC component: the constant I_0, and the triangular component. If a waveform has an AC and a DC part, the two parts are uncorrelated! In fact:

$$i_L = I_{\mathrm{DC}} + I_{\mathrm{AC}}$$

Let's apply the RMS definition on it: the first step was **square**, so:

$$(I_{\mathrm{DC}} + I_{\mathrm{AC}})^2 = I_{\mathrm{DC}}^2 + I_{\mathrm{AC}}^2 + 2I_{\mathrm{DC}}I_{\mathrm{AC}}$$

now, we have to **mean**, and we have three contributes: the integral of a constant, the integral of a variable term, and the integral of the cross-term. As we know, an AC term (like I_{AC}) has the average equal to zero; if we multiply a constant (I_{DC}) for an AC term, we increase the amplitude of the oscillations of the AC term, but keep constant the average, which remains zero! So, in this case:

$$I_{\mathrm{RMS}}^2 = I_{\mathrm{DC}}^2 + I_{\mathrm{AC}}^2$$

Let's apply it to our case:

$$I_{\mathrm{L,RMS}}^2 = I_0^2 + \frac{I_{\mathrm{peak}}^2}{3}$$

where I_{peak} is the distance between the peak and I_0.

Usually, let's note that

$$I_0 \gg \frac{I_{\mathrm{pk}}^2}{3}$$

so:

$$I_{\mathrm{L,RMS}} = \sqrt{I_0^2 + \frac{I_{\mathrm{peak}}^2}{3}} \sim I_{0,\mathrm{RMS}} = I_0$$

We just need, with good approximation, the I_0 term.

Let's consider a numerical example: if $I_0 = 1$ A, with a ripple of $I_{\mathrm{peak}} = 0.3$ A, we have:

$$I_{\mathrm{L,RMS}}^2 = (1\ \mathrm{A})^2 + \frac{(0.3\ \mathrm{A})^2}{3} = 1\ \mathrm{A}^2 + 0.03\ \mathrm{A}^2 = 1.03\ \mathrm{A}^2$$

This means, square-rooting, that:

$$I_{\mathrm{L,RMS}} = 1,015\ \mathrm{A}$$

remembering that Taylor expansion of the square root is

$$(1+x)^{\frac{1}{2}} \sim 1 + \frac{1}{2}x$$

Who cares of 15 mA on 1 A ? No one!

Another way to see this idea, is this one: AC and DC components are orthogonal in Hilbert spaces; we have that the resulting current is very close

to one of the vector of the base of this space (which are the DC and AC components). The diagonal vector, resulting from the linear combination of the two ones, is almost equal to the vertical base element.

In order to design this stuff, we have to calculate some other values: we also need **average values**: in order to calculate them, we have to take the area under the curves, and spread them (like Nutella) on one cycle; as we can see from the graphs, we can calculate the average current as the area of a trapeze:

$$I_{\mathrm{SW,AVE}} = \frac{I_{\max} + I_{\min}}{2} D$$

but we have that:

$$\frac{I_{\max} + I_{\min}}{2} = I_0$$

so

$$I_{\mathrm{SW,AVE}} = I_0 D$$

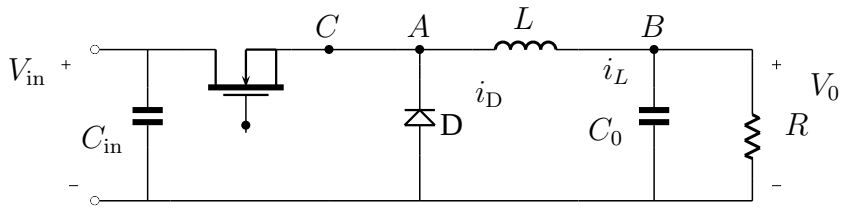
Same thing for the average diode current:

$$I_{\mathrm{D,AVE}} = I_0(1 - D)$$

Why are we using these averages? Why do we need them? Well they are important (as we will see soon) for diodes, BJTs, IGBTs, because the dissipated power P_{diss} on them (approximately) equals:

$$P_{\mathrm{diss}} = V_{\mathrm{D}} I_{\mathrm{D,AVE}}$$

this, for a diode D. This is not important for MOS transistors, because it behaves like a resistor, not like a diode. Same thing for switches: in MOS switches we don't need it! Our circuit will be realized like this one:



In this schematic we have the node C; if we remember that in a (working) capacitor there is no DC, we have that, for KCL, all the average current of the switch must be equal to the input current I_{in}, coming from the supply of the converter; this is normal: the supply gives (approximately) a DC, so we have that:

$$I_{\text{SW,AVE}} = I_{\text{in}}$$

so, the input power of the converter is just equal to:

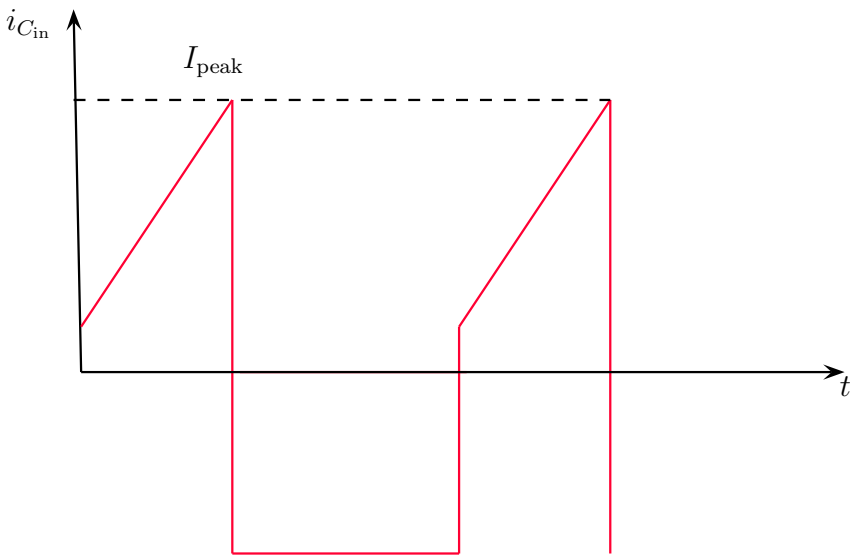
$$P_{\text{in}} = V_{\text{in}} I_{\text{in}} = V_{\text{in}} I_0 D$$

what about output power? Well, trivially, we have:

$$P_0 = V_0 I_0 = V_{\text{in}} I_0 D$$

So, input power and output power are equal; this seems like we have 100% efficiency (but let's remember that our circuit is non-ideal).

Now: we have calculated the average value of the switch (and diode) current in order to calculate the RMS value on the input capacitor. We already said that it is the most stressed, but we have to quantify the stress on it, in order to understand how to design it. We know that the current on the input capacitor C_{in} equals the switch current, less than the DC component.



Can we calculate the RMS value of this graph? Obviously yes, but it can be hard to do: with the definition of RMS value we could calculate it, but we want to do easy things! Remembering the *KCL for RMS values* (which is **not** really a KCL, but only a sort of), we can say that:

$$I^2_{\text{C}_{\text{in}},\text{RMS}} = I^2_{\text{SW,RMS}} - I^2_{\text{SW,AVE}}$$

Of all the RMS value of the switch's current, we take out the average value (which is not into the capacitor), obtaining just the RMS value (RMS value of an average equals the average, because an average is a constant function). So:

$$= I_0^2 D - I_0^2 D^2 = I_0^2 \left(D - D^2\right)$$

the following RMS value quantifies the stress on the input capacitor:

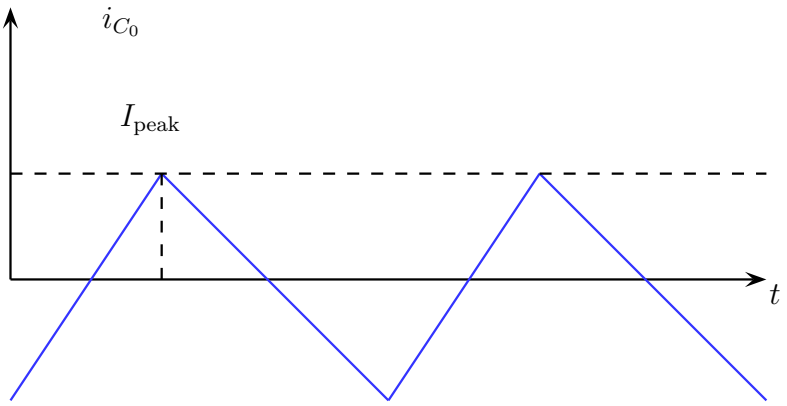
$$I_{\text{C}_{\text{in}},\text{RMS}} = I_0 \sqrt{D - D^2}$$

If we use basic Calculus, we can calculate that the maximum of this function is:

$$I_{\text{C}_{\text{in}},\text{RMS,max}} = \frac{I_0}{2}, \quad \text{for} \quad D = 0.5$$

this is a very important fact.

Let's compare this stress with the output capacitor stress; we know that:



$$I_{\text{pk}} = \frac{I_{\text{max}} - I_{\text{min}}}{2} \ll I_0$$

in fact, the peak is very little respect to the average of the current (which equals the output current): this is an hypothesis of our problem. We know that:

$$I_{\text{C}_0,\text{RMS}} = \frac{I_{\text{pk}}}{\sqrt{3}}$$

This capacitor is less stressed than the input one: it is stressed by a function of I_0, which is very greater respect to the peak value. This occurs because the output capacitor is connected to an inductor: near to an inductor the capacitor has better life, because the inductor can make the current be quite constant (with little ripple); near to a switch, ripple is generally much more higher, so also the stress.

Maximum and minimum of inductor currents

Now, we still have to find the values of I_{max} and I_{min}; as usual, the circuit and the graph of inductor current are:

We already know that:

$$I_0 = \frac{I_{\text{max}} + I_{\text{min}}}{2}$$

We have two unknowns, one equation; the second equation can be something like this one: knowing the slope, and the duration, we can say that the difference between the currents equals the slope, times the duration:

$$I_{\text{max}} - I_{\text{min}} = \frac{V_0}{L}(1 - D)T_{\text{SW}} = \frac{V_0}{L}\frac{1 - D}{f_{\text{SW}}}$$

So, now we have two equations in two unknowns: this is a system! Remembering Ohm's law applied on I_0, we have:

$$\begin{cases} \frac{V_0}{R} = \frac{I_{\max}+I_{\min}}{2} \\ I_{\max} - I_{\min} = \frac{V_0}{L}\frac{1-D}{f_{\text{SW}}} \end{cases}$$

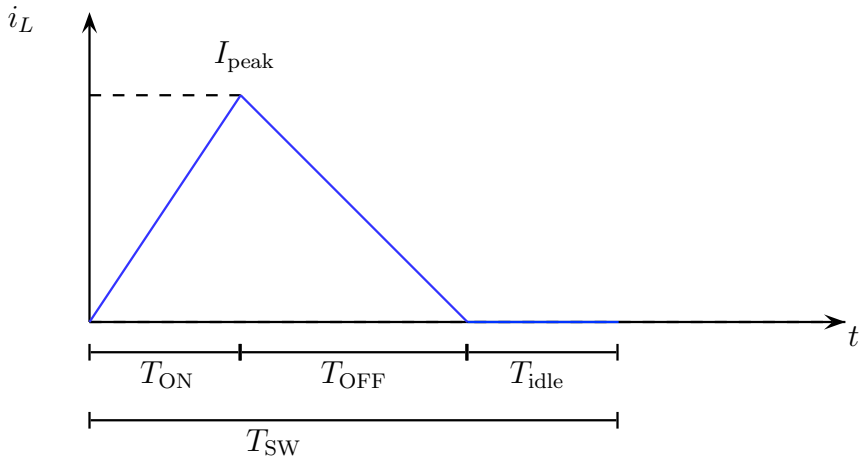
Let's add the two equations: we can obtain (dividing by two):

$$I_{\max} = \frac{V_0}{R} + \frac{V_0}{2Lf_{\text{SW}}}(1-D)$$

Subtracting, we obtain:

$$I_{\min} = \frac{V_0}{R} - \frac{V_0}{2Lf_{\text{SW}}}(1-D)$$

Why do we need those two values? Well, $I_{\max}$ is the peak of the current flowing through all the components! This means that it is related to the peak-stress: we already calculated what happens for average stress (related to RMS value). For the inductor, the peak current is what the inductor dissipates in heat, due to the resistance of the wire which forms the inductor; it is related to the magnetic design of the inductance: the magnetic flux which is inducted into the inductor is related to the R of the inductor, and if we want to find the maximum flux of magnetic field inducted, we need the I_{peak} value, in order to stay away from the saturation of the magnetic core. What about $I_{\min}$? $I_{\min}$ is useful for a different reason: if I make my load lighter, so increase the load resistance, output voltage remains constant, but output current decreases; the output current equals the average inductor current, and ripple is constant (ripple depends just on duty cycle, but not on load resistance); if the load increases too much, $I_{\min}$ touches the zero.



When current becomes zero, the inductor becomes like a short circuit to V_0, the diode opens, and the left side of the inductance hangs on nothing, on an open circuit; this because the diode is reverse biased. Current stays to zero for a while, so comes up, comes down, stays again to zero, and this will be the cycle.

This waveform is different respect to the previous one: we moved from CCM to DCM; the boundary condition from CCM to DCM is $I_{\min} = 0$: when we push $I_{\min}$ to zero, we make our circuit work in DCM.

If we want to design a buck converter in CCM mode, we have to use this idea:

$$I_{\min} = \frac{V_0}{R} - \frac{V_0}{2Lf_{\text{SW}}}(1 - D) = 0$$

$$\Longrightarrow \frac{1}{R} = \frac{1 - D}{2Lf_{\text{SW}}}$$

This is the **only** equation we need to design a buck converter in CCM: this equation says that we have, as degrees of freedom, L and f_{SW}: L is the main degree of freedom we have, because sometimes we have boundaries on f_{SW}. Let's study advantages and drawbacks of high switching frequency:

- if the switching frequency goes up, we can get smaller inductance values, and even better performances (high-frequency inductors are better!); lower switching frequency means larger values of L, and larger size of inductors;
- with higher frequencies we have higher losses: every cycle we lose some energy, so, if we increase the number of cycles, we increase losses;
- in general, one extra condition says that *higher the power, lower the frequency*: larger converters mean larger components: a larger inductor has more parasitic elements, so less bandwidth; if we want to handle high power values, we need larger components; in order to give just an idea about the quantities, we can say that:
  - around 1 kW, switching frequencies can go from 20 kHz to 100 kHz (not under 20 kHz: under 20 kHz we have acoustic frequencies, and acoustic noise produced by our converter: we can hear these noise components!);
  - around 100 W, switching frequencies go from 100 kHz to 500 kHz;

– around 10 W, switching frequencies go from 100 kHz to 1 MHz (but we need different schematics; by the way, at this power level, components are already small, so we don't need to push up too much our frequency).

First thing, to design, is to choose a switching frequency value; in some cases, we have to take pre-defined switching frequencies. For example, if we have to design a switching converter for a TV, if we have to choose a frequency, we want to take a multiple of the display rate: our converter leaks some noise, which goes to the cathodic ray tube; if our noise is fixed, no problem; if our noise moves around the screen, we have to take account of this idea.

Now: chosen the switching frequency with some common sense, the only component we have to design is the inductor! So, we have to find the value of the inductance, given the switching frequency. We have that:

$$\frac{1}{R} = \frac{1-D}{2f_{\text{SW}}L} \Longrightarrow L = R\frac{1-D}{2f_{\text{SW}}}$$

This is the design equation for the buck converter. The L value which satisfies this relation is called L_{critical}: the word *critical* (from the ancient greek $\kappa\varrho\iota\nu\omega$, *divide*), means **separating point**; this means, in this case, the boundary from the DCM to the CCM case. If we want to design in CCM:

$$L > L_{\text{critical}}$$

A remark: L_{critical} is not a well-defined values, because it depends on D and on R: they are not under our control, so we have to calculate the **largest** value of critical inductance (starting from the worst value of D and R): maximum input voltage and minimum load weight correspond to minimum duty cycle and maximum resistance. We have to take also account of the tolerances on the switching frequency: it is realized with non-ideal components (like capacitances and inductors for an oscillator).

Sometimes can happen that the load is disconnected: in this situation, we need an infinite L, in order to remains in CCM; we can have specifications about the load, or about the currents: this means that we have to design the converter in order to remain in CCM with common sense. What we can do is, given the maximum output current, consider as minimum current the 10%, 15%, 20% or something similar, and under this level go to DCM: we can't do anything better with our specifications!

Now, let's consider this fact: we approach DCM when the load resistance goes to maximum value; this rule holds for any converter: when we remove

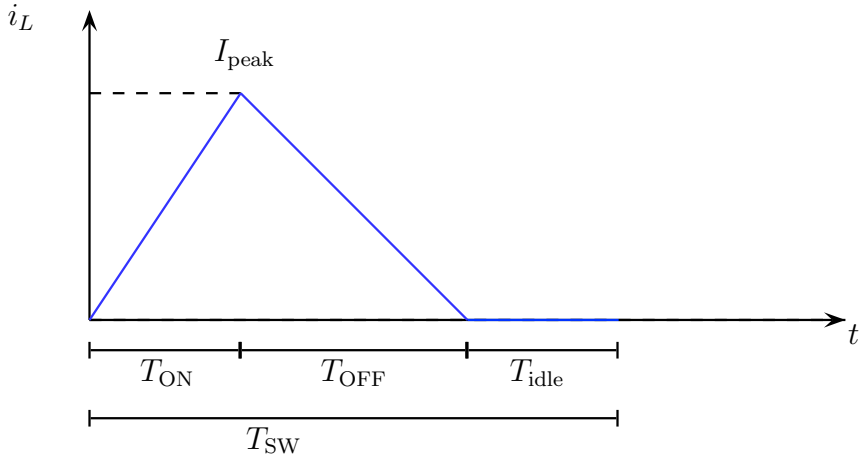
load, we impose DCM. There is a second fact: when input voltage goes up, current decreases, and so we approach DCM; *vice versa*, any converter closed on short circuit works in CCM.

CCM and DCM are also called with other names: CCM is also called **heavy mode**, because related to high current (so heavy loads); DCM is also called **light mode**.

Buck word is related to *money*; another name is **step-down**: given an input voltage, we have, out of it, a lower one; another name, for the same reason, is **chopper** (but this is used from electrotechnicians).

1.2.3 DCM analysis

Let's start to perform a DCM analysis of the buck converter; now our i_L has a different behaviour, respect to the previous one:

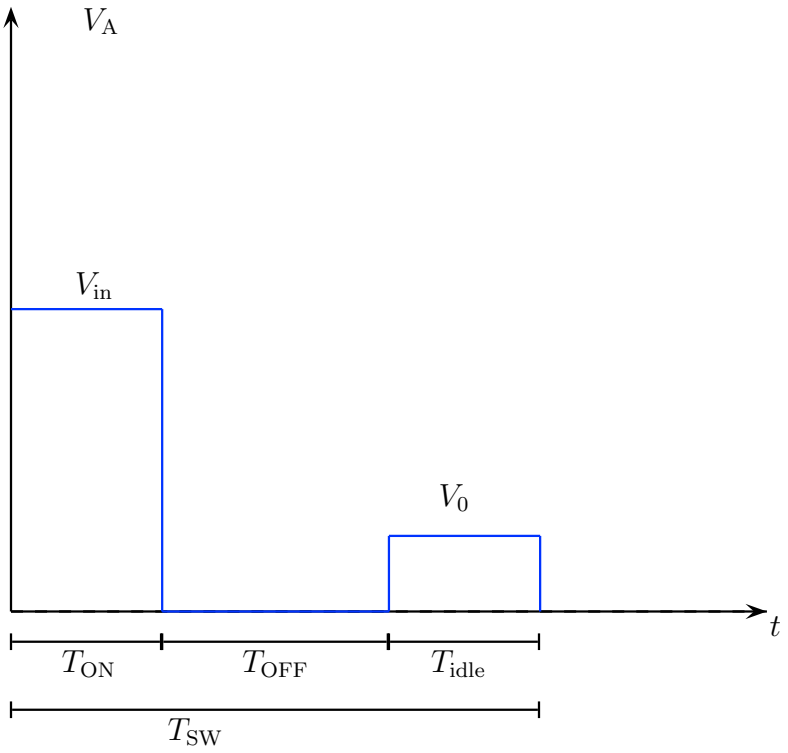


now, there are three times instead of two: T_{ON} (or T_1), T_{OFF} (or T_2), T_{idle} (or T_3): now current ends before the end of the cycle, so T_1 is almost equal to the previous T_{ON}, but the T_2 is not equal to the CCM T_{OFF}: there is a time when current is zero. We have that:

$$T_{\text{SW}} = T_1 + T_2 + T_3$$

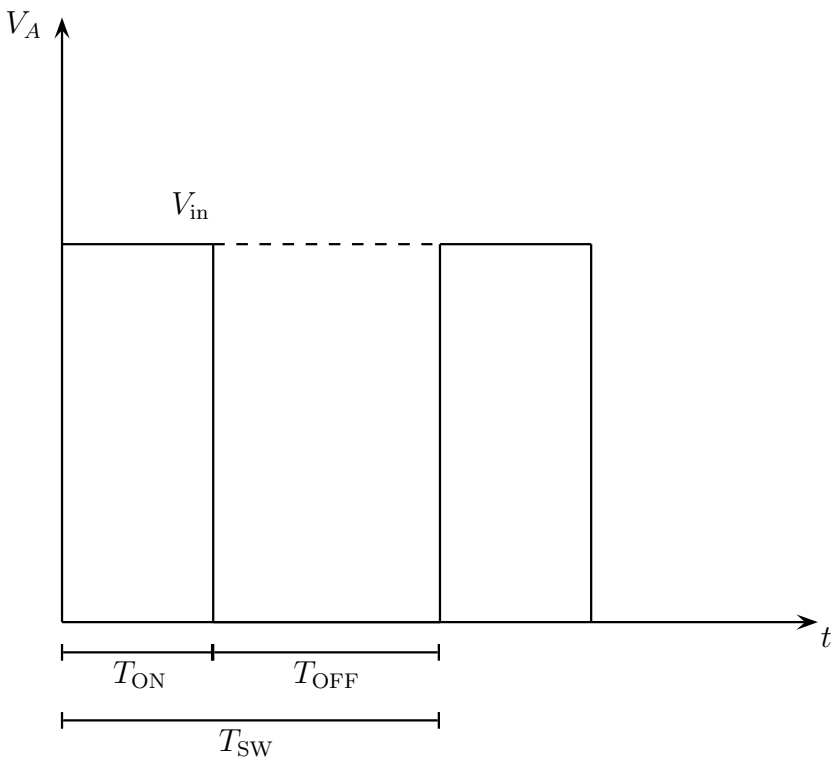
Now, what happens in node A ? Well, if we plot the voltage, we have something like this:

V_A



During T_1 we have V_{in}, during T_2 the voltage drop on the diode (which is considered equal to zero), and on T_3 something new: if the current on the inductor is zero, we have that it behaves like a short circuit, which connects the output voltage to the node A; this is a **step-down** converter, so we suppose that $V_0 < V_{\mathrm{in}}$.

Now, if we use an equivalence, we can model the output with a generic low-pass filter: as any other component it is short-sighted: he doesn't know what is entering: out of it it will produce the average value of what we put in it; in CCM case, we had:



We had this waveform, and now we have another one; the $L - C_0$ block does the average of V_A, so what we have now, with the same D (duty cycle), is a higher voltage respect to the previous case: our actual waveform has higher average value, so, on the load, we will have higher output voltage:

$$M_{\text{CCM}}(D) < M_{\text{DCM}}(D)$$

Where M is defined as:

$$M = \frac{V_0}{V_{\text{in}}}$$

So: the topology is the same of the last time.
We have that positive slope and negative slope are:

$$\left.\frac{\mathrm{d}i_L}{\mathrm{d}t}\right|_{/} = \frac{V_{\text{in}} - V_0}{L}$$

$$\left.\frac{\mathrm{d}i_L}{\mathrm{d}t}\right|_{\backslash} = \frac{-V_0}{L}$$

we have that:

$$\frac{V_{\text{in}} - V_0}{L} T_1 + \frac{-V_0}{L} T_2 = 0$$

and:

$$\frac{V_0}{V_{\text{in}}} = \frac{T_1}{T_1 + T_2}$$

where this fraction is **not** the duty cycle: $T_{\text{SW}} \neq T_1 + T_2$.

We need another equation; one way to obtain it is to look at the output current (there is another way, which will be introduced later): the average current in the capacitor as usually is zero, so we can use the KCL in node A and obtain that $\overline{i_L}$ is the area of the triangle spread (like Nutella!) through T_{SW}:

$$I_0 = \frac{V_0}{R} = \overline{i_L} = \frac{I_{\max}(T_1 + T_2)}{2T_{\text{SW}}}$$

$I_{\max}$ now is quite easy to find: we know that the minimum current is zero, so we can use T_1 and see that:

$$I_{\max} = T_1 \frac{V_{\text{in}} - V_0}{L}$$

substituting:

$$I_0 = T_1 \frac{V_{\text{in}} - V_0}{L} \frac{T_1 + T_2}{2T_{\text{SW}}}$$

now, let's use some algebra: we know that, from the first formula:

$$T_1 + T_2 = T_1 \frac{V_{\text{in}}}{V_0}$$

if we substitute, we obtain:

$$\frac{V_{\text{in}} - V_0}{L} T_1 \frac{T_1 V_{\text{in}}}{V_0} \frac{1}{2T_{\text{SW}}} = \frac{V_0}{R}$$

let's clean this equation:

$$\frac{R}{2LT_{\text{SW}}} T_1^2 \frac{V_{\text{in}}}{V_0} \frac{V_{\text{in}} - V_0}{V_0} = 1$$

but now we have that:

$$\frac{T_1}{T_{\text{SW}}} = D$$

now, so, let's multiply and divide by T_{SW}, and obtain:

$$R\frac{D^2}{2Lf_{\mathrm{SW}}}\left[\frac{V_{\mathrm{in}}}{V_0}\left(\frac{V_{\mathrm{in}}}{V_0}-1\right)\right]=1$$

in these expressions, we have:

$$\frac{V_{\mathrm{in}}}{V_0}=\frac{1}{M}\triangleq\alpha$$

so:

$$\frac{RD^2}{2Lf_{\mathrm{SW}}}\left[\alpha(\alpha-1)\right]=1\Longrightarrow\alpha^2-\alpha-\frac{2Lf_{\mathrm{SW}}}{RD^2}=0$$

this is a second order equation, and is quite different from the CCM: in this expression we have D, but also L, f_{SW}, and the load R: if we change the load, we change the output voltage! The solution of this equation is:

$$\alpha=\frac{1\pm\sqrt{1+\frac{8Lf_{\mathrm{SW}}}{RD^2}}}{2}=\frac{1}{M}$$

so, inverting:

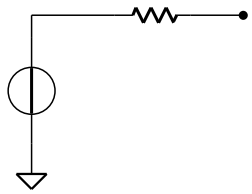
$$M=\frac{2}{1+\sqrt{1+\frac{8Lf_{\mathrm{SW}}}{RD^2}}}<1$$

we have to take just the positive solution, because this number has to be less than 1 (in order to have a buck converter, M can not be greater than 1). If we calculate the limit, we can see that, if $D\to 0$, $M\to 0$: obviously, if we open the switch, output voltage goes to zero, because there is no more input! Let's study the main parameters of this converter, in DCM mode:

- about the output resistance, we have that:

$$\frac{\partial V_0}{\partial I_0}\neq 0$$

  this is non-zero, because output current depends on the load: if we change the load, we have that output voltage changes, so output resistance is not zero. This means that the equivalent circuit for the output stage of the DCM buck converter is something like this:



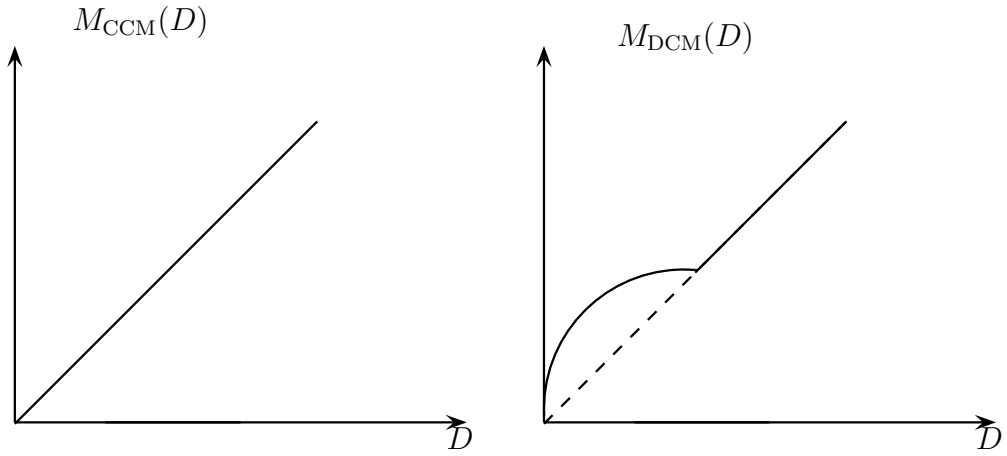
output resistance is not zero, so the load creates a voltage divider;

- as usual, the audio susceptibility is:

$$\frac{\partial V_0}{\partial V_{\text{in}}} = M$$

- about the gain, it is quite complicated to calculate (we have to differentiate respect to D, and it is useless), but we have an information: gain changes with R, so if we change the load, we change the gain. Like previously, the dimension of the gain is **voltage**.

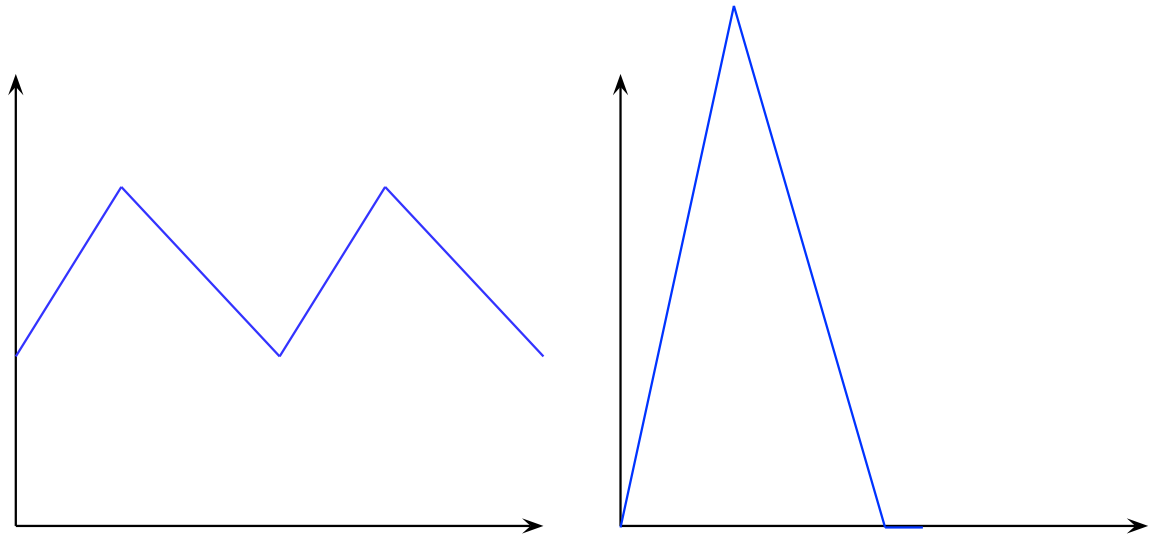
Now, let's graph $M(D)$ in CCM and DCM:



In CCM we have that the derivative of M by D is constant: the curve is a line, so this is obvious; very nice: our gain does not change! In DCM, the situation is much more complicated: we don't have $M = D$, and we have many possibilities, because in DCM there are many parameters which can change: if we change R we change M; the result is that $M_{\text{DCM}}(D)$ has many paths.

There is a common characteristic in all DCM paths: when we increase D, we tend to go from DCM to CCM: this because if we increase the duty cycle, we decrease the input voltage, so we get away from DCM.

Let's do another comparison of CCM and DCM with the same average current:



If we design a CCM converter, the inductor current has just a little ripple, around I_0; in DCM we have to draw a triangle of the same area of the CCM one (the average is equal), so we have a ramp with very high slope; the peak will be very high, and so also RMS value. it is better to use CCM, because it has lower maximum value, and lower RMS values: with CCM our components are less stressed.

When we design a CCM component, we don't have to care about the DCM effect: sometimes we will go in DCM, but when it happens, the average currents will be very different, so also the peaks related to the average currents: DCM is not a problem, from this point of view.

Using the previously seen tricks, we can calculate again the RMS characteristics, and see that:

$$I_{\text{RMS}} = \sqrt{\frac{\frac{T_1+T_2}{T_{\text{SW}}}}{3}} I_{\text{peak}}$$

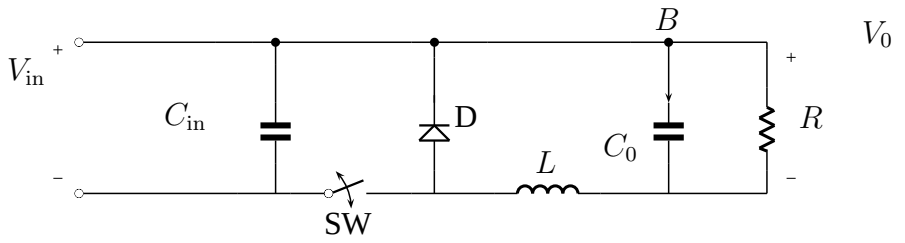
If we know the value of the peak current, and the normalized time (like duty cycle D), we can calculate each value; we know that the current on the inductor is the whole current, and switch and diode are respectively the raising and the falling parts. We can so calculate the stresses of the capacitors, like previously done, with the same ideas.

1.2.4 Alternative schematics for buck converters

Now we are going to show some alternative schematics for buck converters.

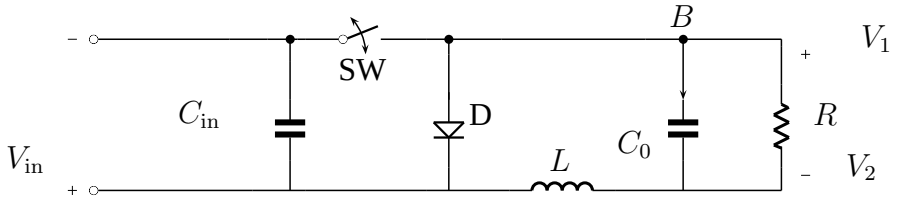
Alternative schematic: components on the *return*

The first idea can be the following one:



Instead of using the standard topology, we can put both switches and inductor in the lower side of the circuit: this is possible because currents, with this idea, follow the same path; this is not very common because, with this graph, input and output positive point are the same (there is a short circuit). The positive voltage is the same all the times, the negative changes, so if we take the output voltage like previously done (from the same pins) the result is the same; if our load is grounded, and also the left part is grounded, maybe to chassis, and our input source is to ground for some other reason, we have a short circuit.

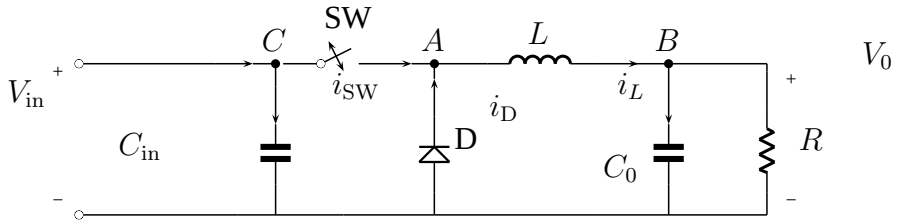
If we use negative input voltage, we can think about something like this:



Let's remember: we don't want to have the switch on one side and the inductor on the other one, because we are not interested to just the differential voltage: output voltage is exactly the same of the previous cases, but we are interested about both differential and common mode voltages, which is very important for electromagnetic compatibility: if we measure V_1 referred to ground, we have that V_1 will be equal to zero, when the switch is closed (in fact, when the switch is closed, the output node is connected to ground via the switch, remembering that now the reference of the supply voltage is in the upper part of the circuit); the capacitor makes voltage be constant on it, so V_2 will go down and up every time V_1 changes its value. This is a source of electromagnetic noise.

High-current schematics

Now: we know that, with new technologies, supply voltages are decreasing, and supply current increasing: in a personal calculator we can have core voltages V_{core} of about 1.1 V, and 90 amps; given a 3.3 V voltage source, we can use a step-down (buck) converter to obtain from the 3.3 V a voltage of 1.1 V; the basic schematic is this one:



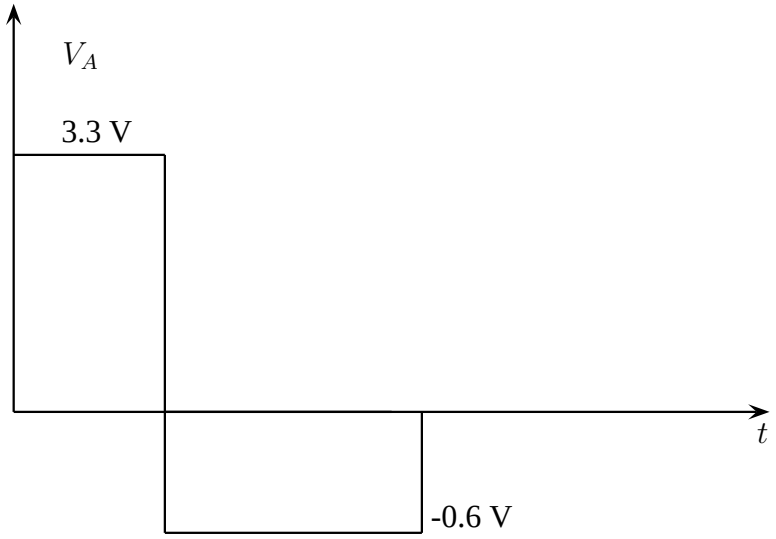
when the diode conducts it can have also 90 A of current inside it! Now, let's do some calculations: if we have to obtain 1.1 V from 3.3 V, we have to design M like:

$$M = \frac{1.1}{3.3} = \frac{1}{3}$$

this means that our duty cycle must be equal to:

$$D = M = \frac{1}{3}$$

What does it means? Well, for $\frac{1}{3}$ of the time we will have our current on the switch, and for $\frac{2}{3}$ of the time on the diode; we have something like this:

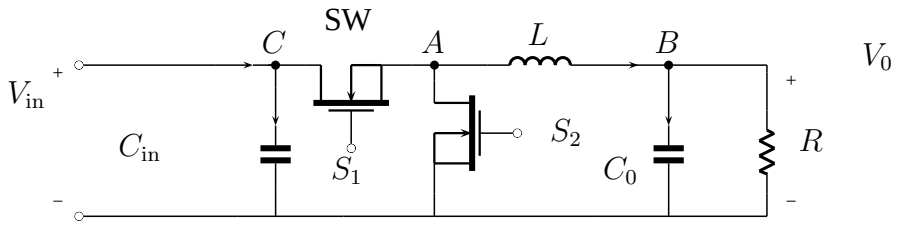


The negative part of this graph generates a lot of losses. Supposing that our diode is a Schottky power diode, with a voltage drop equal to 0.6 V, we have, as dissipated power:

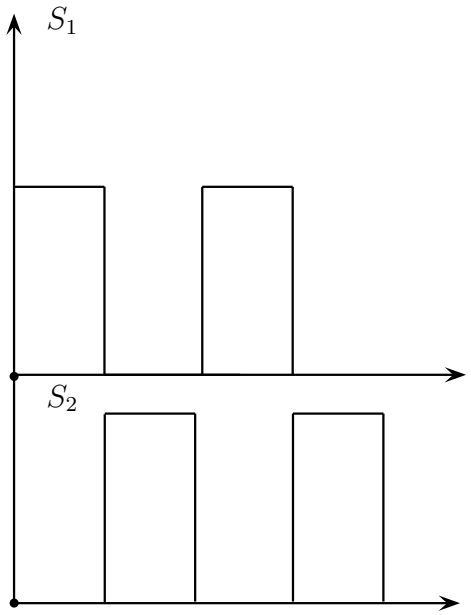
$$P_{\text{diss}} = 90 \text{ A} \times 0.6 \text{ V} \times \frac{2}{3} = 36 \text{ W}$$

so, just on the diode, we are wasting 36 watts! That's a lot of power!

What can we do, to avoid all this power dissipation? Well, we **have to remove the diode**, and to substitute it with something with a similar behaviour: another MOS transistor, working as switch: it has a very low voltage drop! We can't use a bipolar transistor because: *npn* are absolutely forbidden because BJT are unidirectional devices, so an *npn* permits currents to flow just from the collector to the emitter; our idea so can be to put a *pnp* transistor, but there is a problem: surely, if the BJT-switch is closed, current flows in the desired way; if BJT behaves as an open switch, we have that the collector is connected to a high voltage, and so that base-collector is directly biased; the base-emitter junction can not have more that 5 or 6 volt on it, so it can't be use as open circuit. If we put an IGBT instead of a BJT, we have similar problems: also IGBT is unidirectional, but there are some devices with diode included with the main device; our problems come back: a diode has a voltage drop, so wastes power.



This MOS transistor introduces another diode, complimentary, which is perfect for our purposes: it lets current flow from bottom to up; it has low voltage drop and, if it is driven with a correct piloting signal, it can behave like the diode. The idea is to have two signals like these:



With these two non-overlapping signals we can pilot the two switches. This technique is called **synchronous rectification** or **synchronous conversion**: this can be useful every time we have to go down with the output voltage. This technique has many advantages, for example the one that it is **all integrated**: given an IC with the two switches integrated, we have to put just the inductance, and the capacitors (especially the input one).

A final remark: when we are using a synchronous converter, we can make current reach zero, but we can't have DCM: when we put a MOS instead of a diode, it can conduct also *negative currents*, so currents with opposite phase respect to the conventional ones. This, because MOS switches does not open: they conduct, independently on the sign of the current.

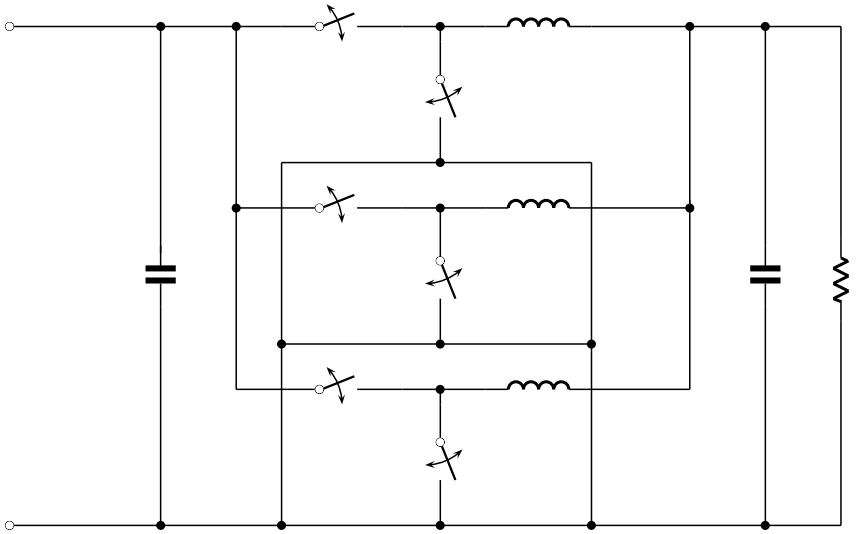
Do we like that these converters stay always in CCM? No: this is not very good, because we have many energy moving from input to output, because of this fact: if current becomes negative, we move energy from output to input; everyone of these movements introduces losses, so we waste energy, and lose efficiency. What we can do in these situations is to emulate a DCM condition, stopping the clock when energy goes back to the input, in order to prevent these losses.

Multi-phase converter

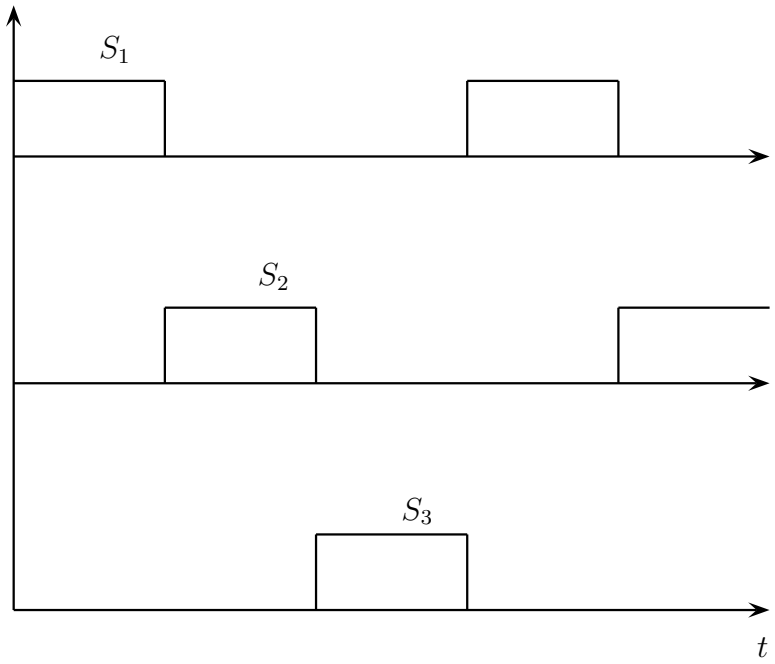
There is another problem: we have to work with currents of about 90 ampere! Currents with these intensities are huge, especially through an inductor!

In order to reduce the stress of all the components, we can use a trick: we know how to realize a buck converter, so, instead of a single converter

which can handle 90 ampere, we can design two or three (we are going to use three) converters, each one handling 30 ampere. This permits to reduce the stresses on the various components.

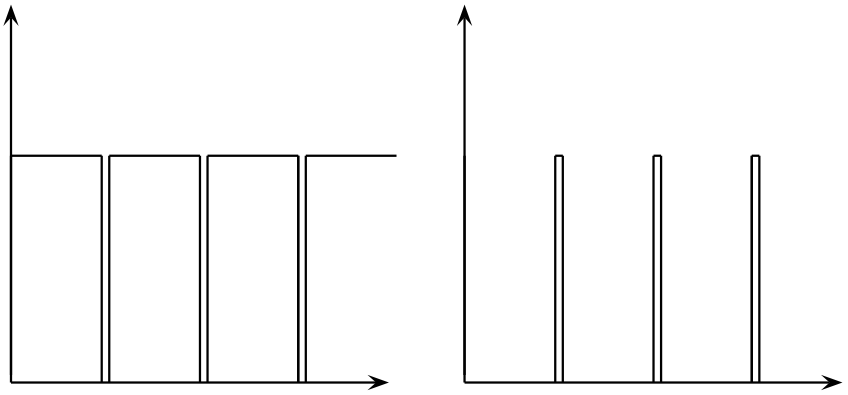


How can we pilot these buck converters in parallel? We have to step down from 3.3 V to 1.1 V, so our signal must have a duty cycle of about $\frac{1}{3}$ (a little bit more or a little bit less); this, for each converter. The difference between the voltages of the converters is this fact: the piloting signals must be delayed of $\frac{1}{3}$ of the time: we have three converters, so the first one will start its work at time 0, the second one at $\frac{T_{\mathrm{SW}}}{3}$, and so on for the third one, which will start at $\frac{2T_{\mathrm{SW}}}{3}$. The three driving signals are the same, delayed! These signals have the same duty cycle, but different phases!



The first converter is driven by S_1, the second one by S_2, the third one by S_3.

What happens with this schematic? Well, in practice, the positive slopes compensate with the negative slopes, so ripple tends to become negligible: if duty cycle is perfect, we have a DC! If duty cycle is slightly more or slightly less, we have something like this:



if duty cycle is slightly less than the right one we have some *drops*, and if we have a duty cycle slightly greater than $\frac{1}{3}$ we have some very narrow peaks. RMS value is small: the RMS value of a DC is the DC (like the previous idea suggests, is like having just one of the vector of the base, with no other contributes from other components!); respect to this value, every variation,

so every AC component, makes the RMS value increase: the minimum value, given a DC, is the DC itself! If RMS value is small, switches, capacitors and inductors are relaxed!

How can this happen? Well, we can use the sort-of-KCL to see that:

$$I_{\text{RMS}}^2 = I_1^2 + I_2^2 + I_3^2$$

It seems that we have to do the sum of the currents, but in this expression we are not taking into account the phase shift! With it, everything becomes ok!

More in general, when we are going to design a multiphase buck converter, we have to use these rules:

1. depending on which voltage level we want to obtain, design the duty cycle, as:

$$D = \frac{V_0}{V_{\text{in}}}$$

2. depending on how many converters we want to use, introduce, from one driving signal to the next one, a phase shift of $\frac{1}{N}$, where N is the number of converters we want to use.

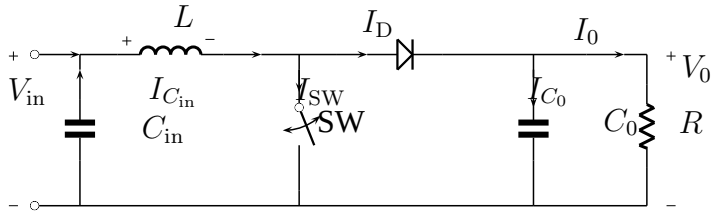
in this example, $D = \frac{1}{3}$, $N = 3$ (but it is a coincidence, that the two numbers are equal).

1.3 Boost converters

Boost converter is the dual of buck converter (we will discuss this statement later):

$$V_0 > V_{\text{in}}$$

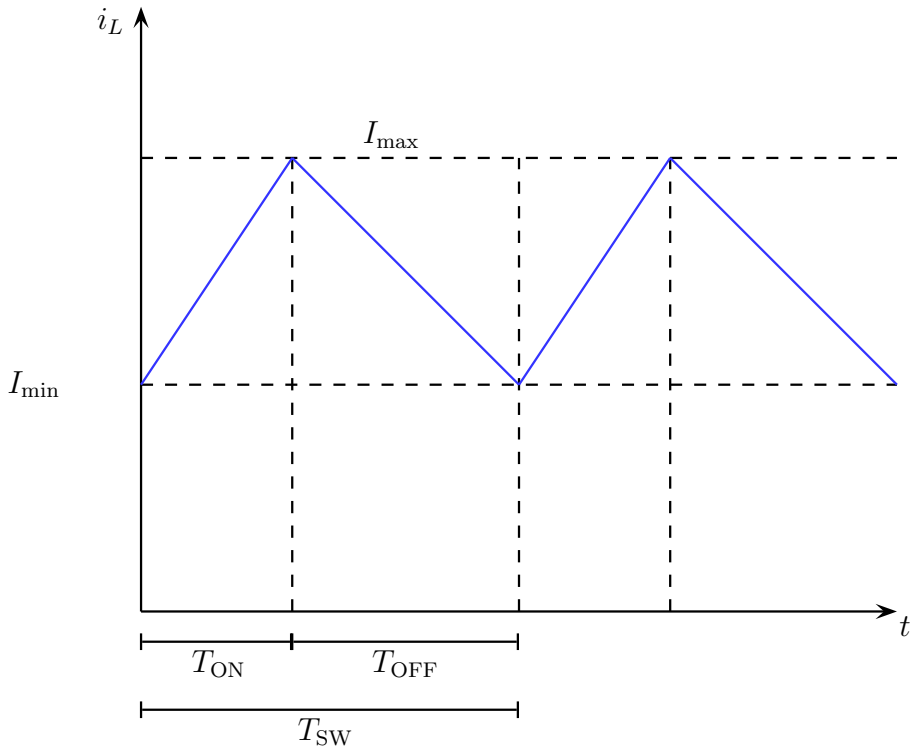
so, we have same polarity, but output voltage larger than input voltage: for this reason, it is also called **step-up**: from an input voltage we have, out of it, a higher one. The basic schematic for this converter is the following one:



this schematic is valid in both CCM and DCM working modes. The input capacitor, as usual, makes our noise to stay into the box, into the circuit.

1.3.1 CCM analysis

As usual, we want to calculate M (so we want to calculate the V_0 over V_{in} ratio) and to find the conditions for stay in CCM/DCM; in order to do it, we can analyze i_L; let's consider the same assumptions we used for buck analysis (we are not going to remember them), and find that:



The waveform is similar to what we have already seen in buck CCM, but with different slopes: now, when the switch is closed (so during $T_{\text{ON}} = T_1$), the voltage on the inductor is equal to V_{in} (we are ignoring the voltage across the switch); so:

$$\left.\frac{\mathrm{d}i_L}{\mathrm{d}t}\right|_{\nearrow} = \frac{V_{\text{in}}}{L}$$

What about $T_{\text{OFF}} = T_2$, when the switch is open? Well, we have that the left pin of the inductor is connected to V_{in}, and the right one to V_{out}, thanks to the diode (supposing that it's ideal):

$$\left.\frac{\mathrm{d}i_L}{\mathrm{d}t}\right|_{\backslash} = \frac{V_{\mathrm{in}} - V_0}{L}$$

Now, remembering what we have done for buck converter, we impose the cyclostationary condition, and obtain:

$$\frac{V_{\mathrm{in}}}{L} T_1 + \frac{V_{\mathrm{in}} - V_0}{L} T_2 = 0$$

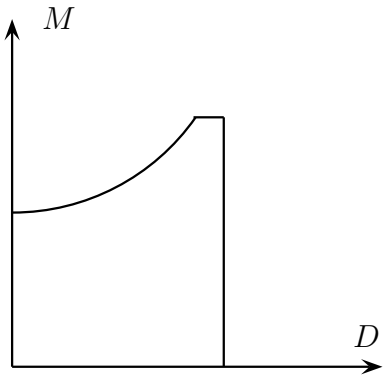
this can be solved as:

$$V_{\mathrm{in}} \left(T_1 + T_2\right) = V_0 T_2$$

so:

$$\frac{V_0}{V_{\mathrm{in}}} = \frac{T_1 + T_2}{T_2} = \frac{T_{\mathrm{SW}}}{T_2} = \frac{1}{1 - D}$$

This is our converter; the minimum value of the output voltage is for $D = 0$, and it is V_{in}: if $D = 0$, this converter behaves like a piece of wire. If $D \to 1$, we have a behaviour like this:



This, because if we have $D \to 1$, we have that the switch stays closed, so the output voltage decreases because the output capacitance discharges on the load, and voltage continues to decrease.

Let's calculate our parameters: we have that:

$$V_0 = \frac{V_{\mathrm{in}}}{1 - D}$$

- about the output resistance, we have that:

$$\frac{\partial V_0}{\partial I_0} = 0$$

we don't have I_0 dependency in our equation, so output resistance is zero!

- as usual, the audio susceptibility is:

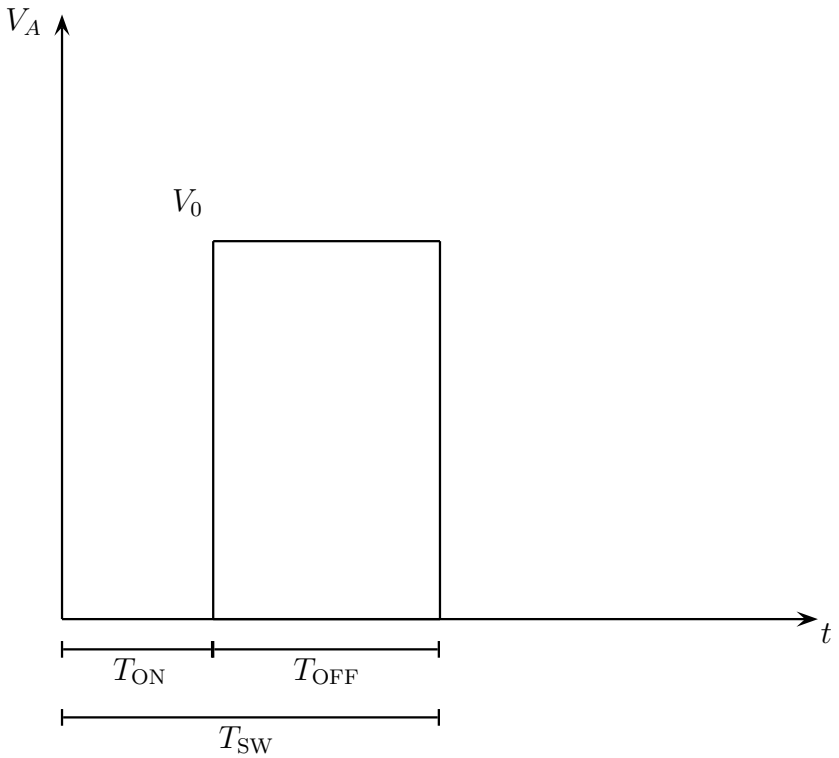
$$\frac{\partial V_0}{\partial V_{\text{in}}} = M$$

- about the gain:

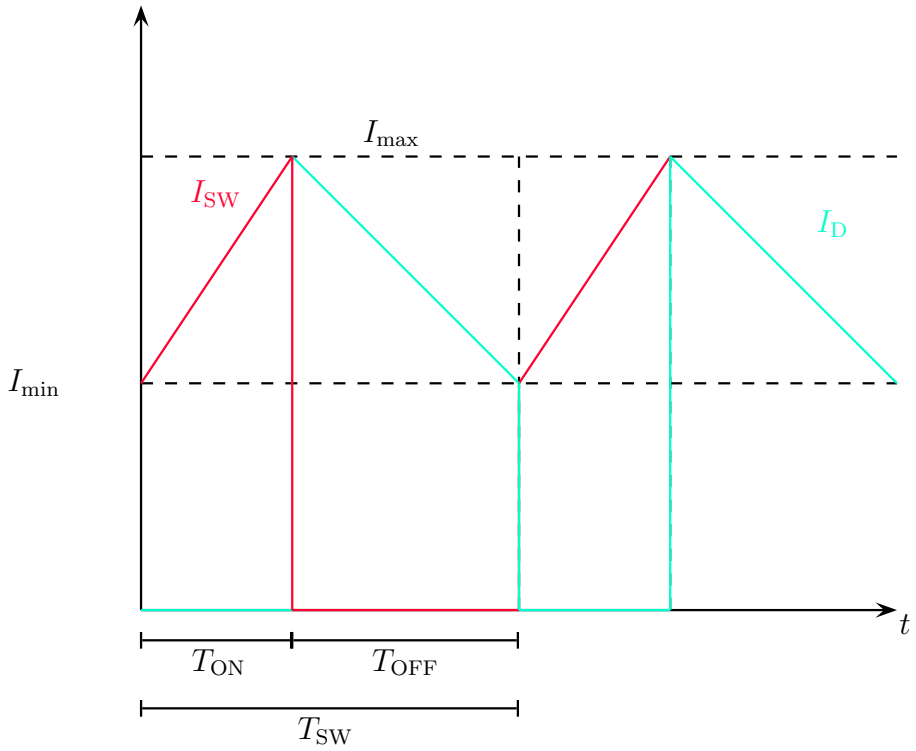
$$\frac{\partial V_0}{\partial D} = \frac{V_{\text{in}}}{(1-D)^2} = \frac{V_0}{1-D} = \frac{V_0^2}{V_0(1-D)} = \frac{V_0^2}{V_{\text{in}}}$$

in buck converter we had V_{in}, but now we have a strong dependency on the output voltage: this is dual to it!

Now, let's find the various parameters we need to calculate the stresses: let's start from V_A:

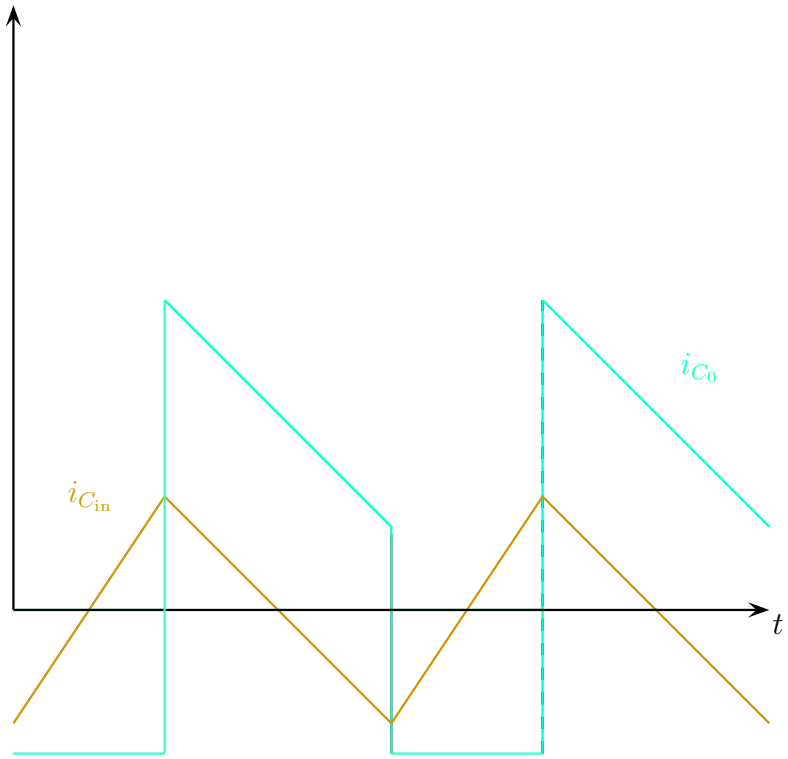


Then, it's i_{SW} turn: it is the current flowing on the switch, so it is equal to the inductor current, when the switch is closed; zero, when it is open. In a dual way, i_{D} is the current flowing into the diode, when the switch is open, so it is equal to i_L, when the switch is open:



Now, in order to quantify the stresses, we have to calculate the currents on C_{in} and C_0:

- $i_{C_{\mathrm{in}}}$ is the inductor current, minus its average (which we will calculate later);
- i_{C_0} is the diode current, without its average.



The most stressed component, as we can see, is the output capacitor: surely it will have the greater RMS value.

Now, let's find some values: first of all, I_{min} and I_{max}.

We already need two equations: the former one, and the fact that:

$$I_{\text{max}} - I_{\text{min}} = \frac{V_{\text{in}}}{L} T_1$$

or

$$I_{\text{max}} - I_{\text{min}} = \frac{V_0 - V_{\text{in}}}{L} T_2$$

and, we have that the average value of I_{max} and I_{min} is:

$$\frac{I_{\text{max}} + I_{\text{min}}}{2} = I_{\text{in}}$$

This is different from what we seen in buck converter: now, the average of the inductor current is equal to the input current, not to the output current. We prefer to refer this equation to the output current, because we can use Ohm's law and refer it to the output voltage; we know that, if all components are ideal, output power equals input power, so that:

$$V_0 I_0 = V_{\text{in}} I_{\text{in}}$$

but we know that

$$I_0 = \frac{V_0}{R}$$

so:

$$I_{\text{in}} = \frac{V_0^2}{V_{\text{in}}} \frac{1}{R} = \frac{V_0}{(1-D)R}$$

Our two equations are:

$$\begin{cases} I_{\max} - I_{\min} = \frac{V_{\text{in}}}{L} T_1 = \frac{T_1 V_0 (1-D)}{L} \\ I_{\max} + I_{\min} = \frac{2V_0}{(1-D)R} \end{cases}$$

So, the solutions for this system are:

$$I_{\max} = \frac{V_0}{(1-D)R} + \frac{T_1 V_0 (1-D)}{2L}$$

$$I_{\min} = \frac{V_0}{(1-D)R} - \frac{T_1 V_0 (1-D)}{2L}$$

If we multiply and divide by T_{SW}, we obtain two more interesting equations:

$$I_{\max} = \frac{V_0}{(1-D)R} + \frac{V_0 D (1-D)}{2L f_{\text{SW}}}$$

$$I_{\min} = \frac{V_0}{(1-D)R} - \frac{V_0 D (1-D)}{2L f_{\text{SW}}}$$

Now, let's use them. Now, we want to find the boundary condition which ensures to work in CCM; in order to do it, let's put $I_{\min}$ equal to zero:

$$I_{\min} = \frac{V_0}{(1-D)R} - \frac{V_0 D (1-D)}{2L f_{\text{SW}}} = 0$$

As usual, the degree of freedom of this equation are L and f_{SW}; supposing that, from the specifications on power we have chosen f_{SW}, the most useful form for this equation is the one who uses L as unknown:

$$L_{\text{critical}} = \frac{(1-D)^2 R D}{2 f_{\text{SW}}}$$

now:

- if $L > L_{\text{critical}}$ we are sure to work in CCM;
- if $L < L_{\text{critical}}$ we are sure to work in DCM.

Obviously, of all the possible values of L_{critical}, we have to choose the one which ensures our condition; this can be found using the maximum load resistor R (for whom the output current becomes minimum), and some particular value for D. Which value? Well, this is not trivial as it was for buck converter: we have to differentiate the function respect to D, and obtain:

$$\frac{\mathrm{d}L}{\mathrm{d}D} \propto \left[(1-D)^2 - 2D(1-D)\right] = 0$$

$$\Longrightarrow = (1-D)\left(1-D-2D\right)$$

this is satisfied when:

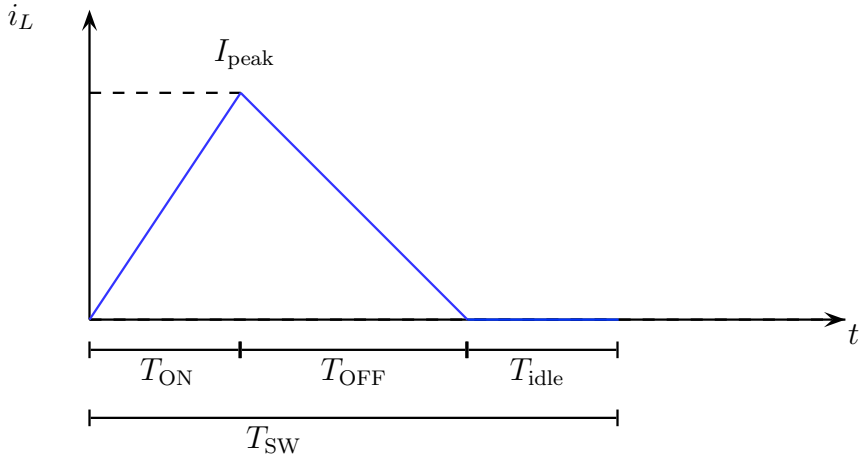
$$D = 1 \quad \text{or} \quad D = \frac{1}{3}$$

We have to take the maximum value to stay in CCM, but it depends on the D range we have. Remembering that our maximum is $D = \frac{1}{3}$ (the other one is a trivial solution for a minimum), we can be sure to be in CCM.

For reasons we will explain later, sometimes we need to design boost converters in DCM; in order to do it, we have to use an inductance value which must be less than the L_{critical} value; the minimum value of L_{critical} needs minimum R, and about D, try to minimize it (studying the curves).

1.3.2 DCM analysis

The graph of i_L current, in DCM, is something like this:



Now, we want to find all our parameters, for DCM; first of all, M:

$$M = \frac{V_0}{V_{\text{in}}}$$

Now, if we take $L < L_{\text{critical}}$, we are almost sure to be in DCM. Let's remember the already-find equation:

$$\frac{V_0}{V_{\text{in}}} = \frac{T_1 + T_2}{T_2} = \frac{T_1}{T_2} + 1 = M_{\text{DCM}}$$

Let's remark that $T_{2,\text{DCM}}$ is shorter than $T_{2,\text{CCM}}$, because now we have also the idle time T_3; we can say that:

$$M_{\text{CCM}} < M_{\text{DCM}}$$

Now, we need another equation: we have two unknowns, and just one equation; this can be find using the Ohm's law applied to the output, related with the average diode current (now output current is related with diode current, not with inductor current):

$$\frac{V_0}{R} = \overline{i_{\text{D}}}$$

Now, we have that the average of the diode current is equal to the area of a triangle, spread on the entire T_{SW}; this means that, given T_2 as base, and $I_{\max}$ as height

$$\overline{i_{\text{D}}} = \frac{1}{2}\frac{1}{T_{\text{SW}}} T_2 I_{\max}$$

so, our two equations are:

$$\begin{cases} \frac{V_0}{R} = \frac{1}{2}\frac{T_2}{T_{\text{SW}}}\frac{V_{\text{in}} T_1}{L} \\ M = \frac{V_0}{V_{\text{in}}} = 1 + \frac{T_1}{T_2} \end{cases}$$

from the second equation, we can find (inverting it) that:

$$T_2 = \frac{T_1}{M - 1}$$

substituting:

$$\frac{V_0}{V_{\text{in}}} = M = R\frac{1}{2}\frac{T_1}{T_{\text{SW}}}\frac{1}{M-1}\frac{T_1}{L}$$

But we have that

$$\frac{T_1}{T_{\mathrm{SW}}} = D$$

So, multiplying and dividing as usual for T_{SW}, we obtain:

$$M(M-1) = \frac{RD^2}{2Lf_{\mathrm{SW}}}$$

this is a second order equation:

$$M^2 - M - \frac{RD^2}{2Lf_{\mathrm{SW}}} = 0$$

its solutions are:

$$M = \frac{1 \pm \sqrt{1 + 2\frac{RD^2}{f_{\mathrm{SW}}L}}}{2}$$

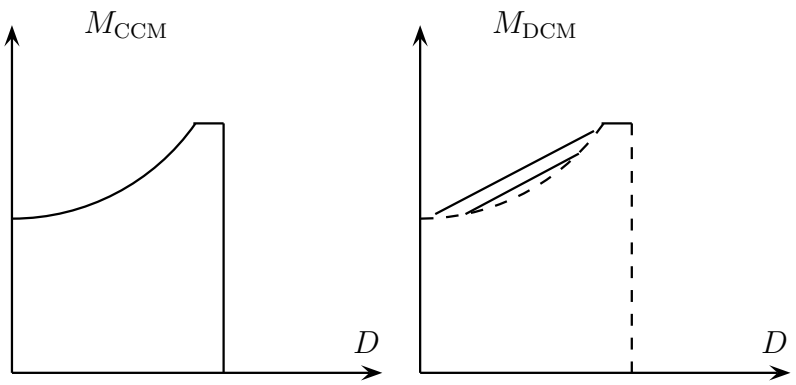
we want the positive solution, in order to have M larger than one:

$$M = \frac{1 + \sqrt{1 + 2\frac{RD^2}{f_{\mathrm{SW}}L}}}{2}$$

Some observations about the parameters (we are not going to calculate or show them):

- the output resistance is different than zero, because we have dependency on the load;
- as usual, the audio susceptibility is equal to M;
- the gain has a complicated expression (which can be found by differentiating the expression by D), but this is not interesting; it is, dimensionally, a voltage.

If we want to graph the behaviour of M in CCM and DCM, we obtain something like this:



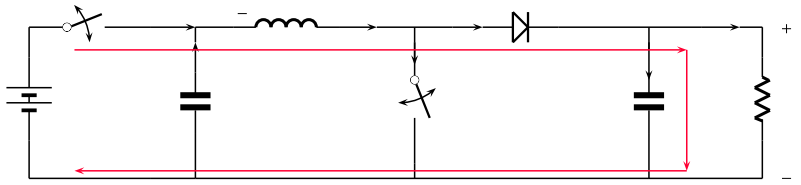
In CCM we have the already-known result; in DCM, we have something almost similar to straight lines: they are not really lines, but something similar; at start we have CCM, so DCM, and then again CCM.

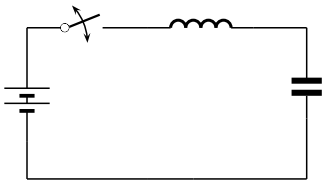
Now, few more observations: if $R \to \infty$, we have that M_{DCM} goes to infinite: this means that if we are working with an open loop converter, so without a control, if we disconnect the load, we break the boost converter (or its protections): we **must avoid to disconnect the load**.

For buck converters, we preferred CCM, because the various components were less stressed: if we have two converters handling the same powers, one designed in DCM and one in CCM, the one in DCM will have higher RMS values for each component (and this is really bad!). This was true for buck, but it is also true for other converters.

Unfortunately, CCM is almost impossible to control, in boost converters, so we have to stay in DCM: CCM transfer function (in Laplace domain) has a zero in the right half-plane, so it is almost impossible to control; DCM means to have stressed components, and less available power; this means that, if we want to design a step-up converter, the best idea (with our actual knowledge) is to use a buck converter with a transformer, in order to handle both voltage and power. We will study these phenomena later, when we are going to show how to control these converters.

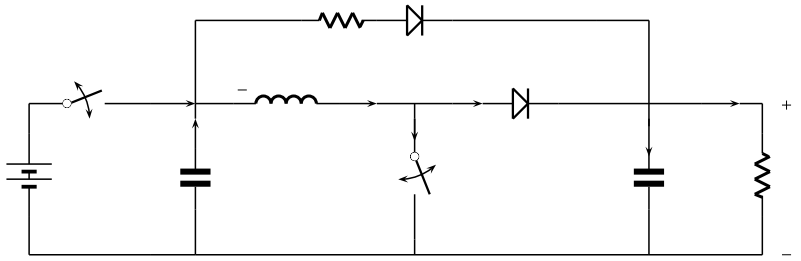
Boost converter has other issues: if we have a boost converter like this, with high load:





The mesh behaves as a resonant circuit!

In fact, we still have the diode, which blocks current to flow in the opposite verse, and maintains the current positive, so the voltage equals the peak value: the load is light, so it steals a little current from the resonant circuit, and the diode doesn't permit to the sine wave to come down. From one side, we are boosting the value, so the circuit behaves as a boost converter, because the output voltage goes to $2v_{\text{in}}$. Sometimes we just want a high voltage value, but if our output voltage must be precise, this resonance is a problem! How to solve it? Well, we can use this idea:

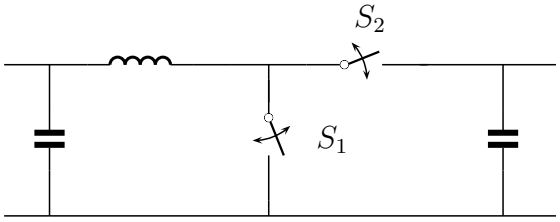


Resonance can be removed by introducing losses into our circuit! But... We can't introduce losses, because they reduce η! What to do? The standard solution is to put a resistance in parallel of the mesh, and a diode: the diode prevents the added resistance to conduct when the converter is working! This means that this resistance works just during the transient, and its work is just to charge the capacitor. The value of this resistance is:

$$R < \sqrt{\frac{L}{C_0}}$$

1.3.3 Synchronous boost converter

Can we realize a synchronous boost converter? Of course, yes:



Now, just a remark: if we read this circuit from left to right, this is a boost converter; if we read it from right to left, this is a buck! This means that a synchronous buck (or boost) converter is a bidirectional circuit: seen from one side is a buck, from the other a boost. We have:

$$\left.\frac{V_2}{V_1}\right|_{\text{boost}} = \frac{1}{1 - D_{\text{S1}}}$$

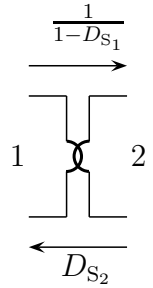
$$\left.\frac{V_1}{V_2}\right|_{\text{buck}} = D_{\text{S2}}$$

So, if we remember that:

$$D_{\text{S1}} = (1 - D_{\text{S2}})$$

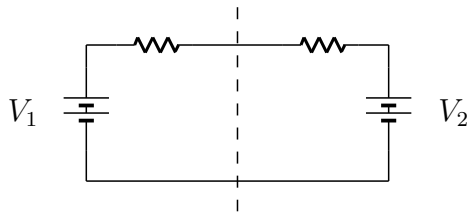
these two parameters, two normalized times, are the same! This means that we can see the two circuits as a single circuit, remembering the relations between the duty cycles, and considering as T_{ON} for the interesting point of view (buck or boost), so as D_{i}, the signal which keeps closed the switch of the converter (remembering to consider that the other one is just a substitute of the diode).

We can do an observation: this converter, basically, acts like some kind of transformer!

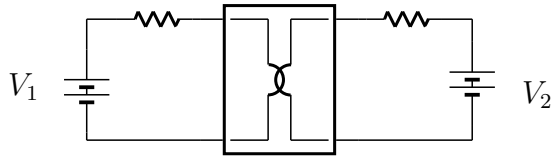


This is a special transformer: it is able to transform DC: it has no magnetic core limitation, so its bandwidth starts from $s = 0$! We can see that it behaves, depending on the direction, as written.

Now, let's consider this basic circuit:

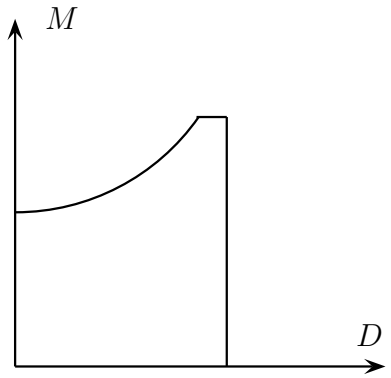


Which is the power flow of this converter? Well, it depends on the highest voltage level: in fact, the highest value of voltage decides the verse of the power (left to right or right to left); if we do something like this:

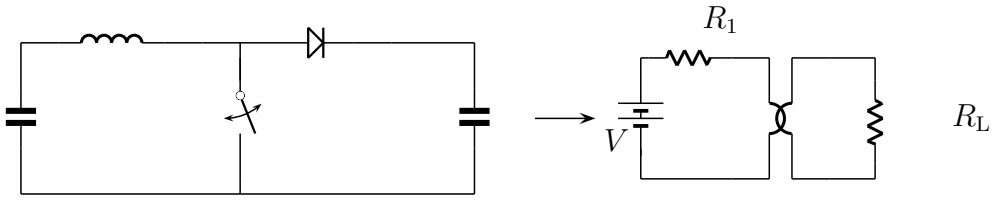


This can change voltage and resistance seen from the pins, so also the power flow: we can move energy to the direction we want.

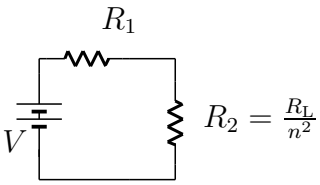
We said that our circuit has a behaviour like this:



If we think at the boost converter as a DC transformer, it is easy to understand why we have something like this: we have non-ideal components; for example our inductor will have a series resistance, so we get this situation:



Taking out of the circuit all the boost schematic and introducing just the transformer symbol, we obtain this:



by changing the duty cycle D, we can obtain a resistance R_2, from R_L, and its value depends on the parameter n of the converter. R_1 is the combination of all loss resistances (source, capacitors, inductor etc.).

Let's look at the maximum output power: for this circuit we can easily proof (by computing i and v, multiplying, differentiate and put to zero) that we have the maximum output power when:

$$R_1 = R_2 = \frac{R_L}{n^2}$$

If we maximize the output power, the maximum efficiency is equal to 50%: this is a bad condition for a DC-DC converter!

From this condition, if we want to get higher output voltage values, what we obtain is something very bad: when we are increasing voltage, we find a maximum, and if M keeps going larger and larger (trying to increase output voltage), we go from the other side of the maximum:

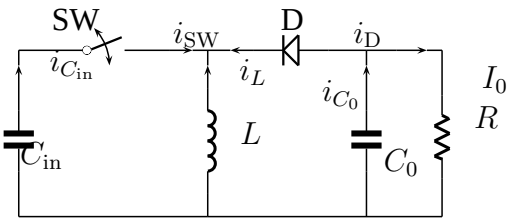
if we go to the other side of the maximum, the slope changes, and this means having a sort of amplifier with a negative gain! In fact:

$$\frac{\partial V_0}{\partial D} = \text{gain}$$

This is very bad: boost converter must be controlled, so it is inside a closed loop! If we introduce a negative sign, we change the phase of 180°, and this makes the feedback be a positive feedback: as we try to increase the output voltage, by increasing M, we decrease it, due to the negative slope, so the control goes in panic!

1.4 Buck-boost converters

Buck-boost converter topology is something like this:



This was formerly invented as an autonomous converter: this is one of the oldest converters, and for many years it was considered as a basic topology; actually, we know that it is composed from a buck, and a boost (we will discuss this later).

An observation: the input has a switch, the output a diode: the first observation is that it has the input of a buck converter and the output of a boost converter; we are going to analyze M:

$$M = \frac{V_0}{V_{\text{in}}}$$

1.4.1 CCM analysis

Let's start as usual with i_L, using the standard hypothesis: i_L starts from a non-zero $I_{\min}$ value, after a time T_{ON} (time when the switch is closed) it reaches a maximum current value $I_{\max}$, then it starts decreasing, continues for a time T_{OFF} (when the switch is open), and goes back to $I_{\min}$ (this, because we are imposing the cyclostationary condition).

By studying this topology, we can see that:

$$\left.\frac{\mathrm{d}i_L}{\mathrm{d}t}\right|_{/} = \frac{V_{\text{in}}}{L}$$

$$\left.\frac{\mathrm{d}i_L}{\mathrm{d}t}\right|_{\backslash} = \frac{V_0}{L}$$

An observation: buck-boost converter is an **inverting** converter: we have that $V_0 < 0$, so slope is negative even if the sign is not showed, because of this reason.

Our equation is:

$$\frac{V_{\text{in}}}{L}D + \frac{V_0}{L}(1-D) = 0$$

from here, with some algebra, we can obtain:

$$\frac{V_0}{V_{\text{in}}} = -\frac{D}{1-D}$$

this is normal: we have a **negative output voltage**, assuming to have a positive voltage: $V_{\text{in}}V_0 < 0$!

Another remark: this expression can go from 0 to ∞; as engineers we must know that the infinite does not exist, so this expression will reach some maximum. Output voltage can be higher or lower, in modulus, respect to the input one.

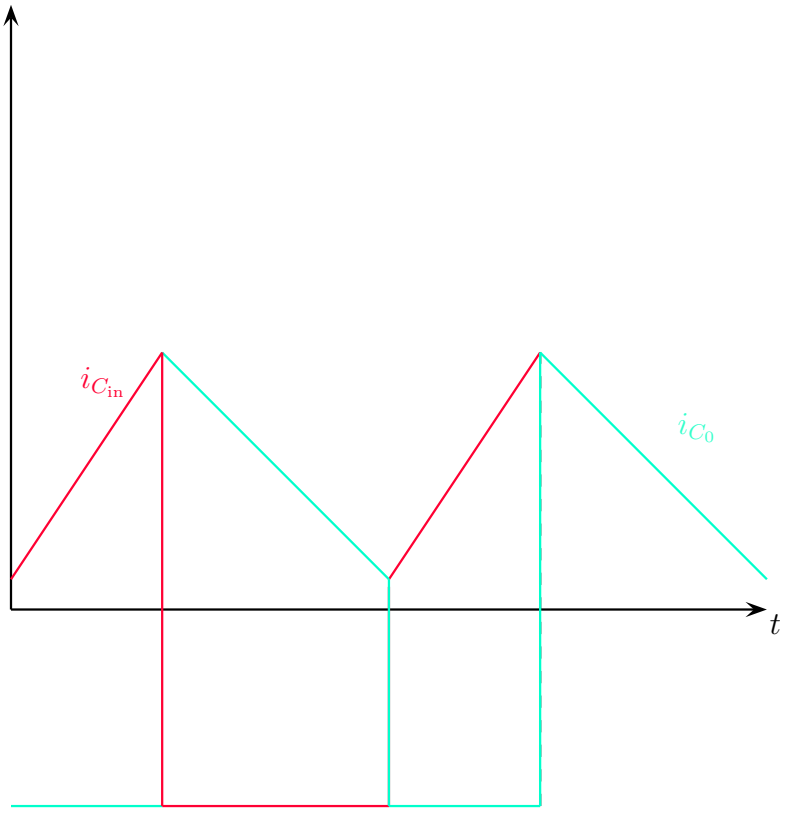
Now, the same, standard stuff: let's see that i_{SW} is the current flowing through the inductor during T_{ON} (or D, using normalized values respect to the full switching time T_{SW}), and i_{D} is the current through the diode when the switch is open.

Bad news: both input and output capacitors are very stressed, because on them there is a pulsed current, so its RMS value will be very high. The currents through the two capacitors in fact are:

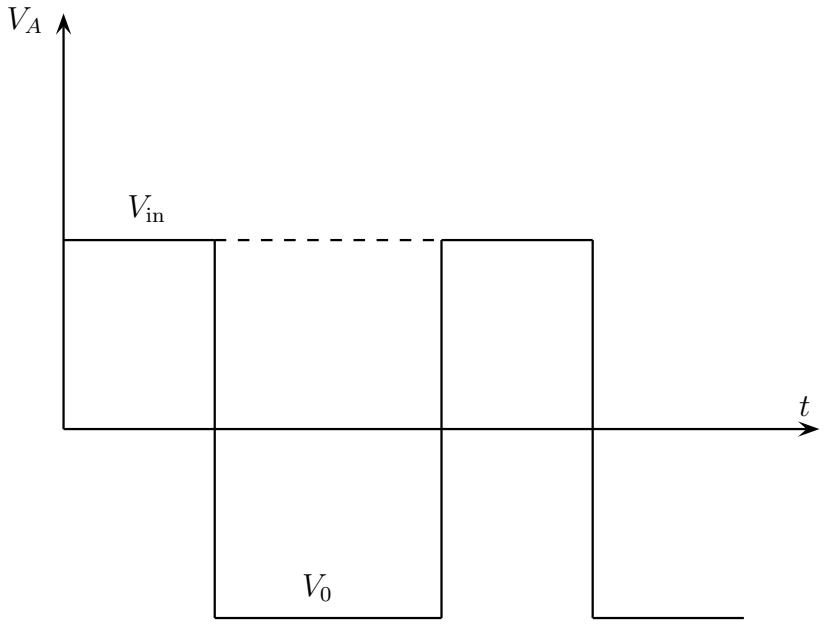
$$i_{C_{\text{in}}} = i_{\text{SW}} - I_{\text{IN}}$$

$$i_{C_0} = i_{\text{D}} - I_0$$

and we have graphs like these:



Now, what else? Well, voltages! The only interesting node is the node A, so the voltage on it is something like this:



during T_{ON} the switch is closed, so we have V_{in}; during T_{OFF}, we have V_0: let's remember that the two voltages have different signs, so we have a spreading from a positive V_{in} to a negative V_0: this is a high voltage stress! We have to take account on it, when we are going to choose the diode and the switch: they must survive after this voltage change!

In DCM, everything is worst, as usual, so we want to work in CCM, unfortunately this is almost impossible, because, as the boost converter, this has control issues: we have to design it in DCM. All the SoB (Son of a Boost) converters have the same issue.

Now, let's calculate I_{min} and I_{max}: as usual, we need two quantities, and two equations. The first one is:

$$I_{\text{max}} - I_{\text{min}} = -\frac{V_0}{L} T_{\text{OFF}} = -\frac{V_0}{L} \frac{1-D}{f_{\text{SW}}}$$

let's remember that $V_0 < 0$ for hypothesis!

Once more, we need the average of the two currents: the average of I_{min} and I_{max}, as usual, is just the average value through the inductor. What we can't do is to relate directly to V_0: now the output current is related to the DC value of the diode current, not of the inductor's one; what we can do is see that:

$$\overline{i_{\mathrm{D}}} = \frac{I_{\max} + I_{\min}}{2}(1-D)$$

this, because we are spreading the area of the trapezoidal waveform through a cycle!

so:

$$-\frac{V_0}{R} = \frac{I_{\max} + I_{\min}}{2}(1-D)$$

we related the output current to the diode current, but the result is the same: we have our equation! The system we have to solve is:

$$\begin{cases} I_{\max} - I_{\min} = -\frac{V_0(1-D)}{Lf_{\mathrm{SW}}(1-D)} \\ I_{\max} + I_{\min} = -\frac{V_0}{R}\frac{2}{1-D} \end{cases}$$

so, by adding and subtracting the two equations, we obtain:

$$I_{\max} = -\frac{V_0}{R(1-D)} - \frac{V_0}{2Lf_{\mathrm{SW}}}(1-D)$$

$$I_{\min} = -\frac{V_0}{R(1-D)} + \frac{V_0}{2Lf_{\mathrm{SW}}}(1-D)$$

The first one is useful to calculate the stresses on the components; the second one is useful in order to find the DCM/CCM boundary condition: if we put $I_{\min} = 0$:

$$-\frac{V_0}{R(1-D)} + \frac{V_0}{2Lf_{\mathrm{SW}}}(1-D) = 0$$

this means:

$$\frac{1}{R(1-D)} = \frac{1-D}{2Lf_{\mathrm{SW}}}$$

as usual, we decide and fix a value for f_{SW}, and find L:

$$L_{\mathrm{critical}} = \frac{(1-D)^2 R}{2f_{\mathrm{SW}}}$$

This is again the critical value for L, the boundary condition. Like usual, it is a variable value, so if we want to stay in CCM, we have to satisfy this condition for the maximum critical inductance: this is the one with maximum load resistance, and with the minimum D: we have that

$$M = \frac{D}{D-1}$$

so, this is a monotonic function; the minimum duty cycle brings the maximum current!

Now, let's calculate the three parameters:

$$\frac{\partial V_0}{\partial I_0} = 0$$

$$\left.\frac{\partial V_0}{\partial V_{\text{in}}}\right|_{D=\text{constant}} = M$$

this is the same result of all times; so, by computing the derivative respect to D of V_0:

$$\frac{\partial V_0}{\partial D} = \frac{-V_{\text{in}}}{(D-1)^2}$$

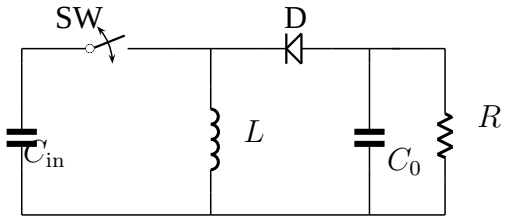
or, in a different way:

$$= -\frac{D}{D(D-1)^2}V_{\text{in}} = -\frac{V_{\text{in}}D}{D(D-1)(D-1)} = \frac{V_0}{D(D-1)}$$

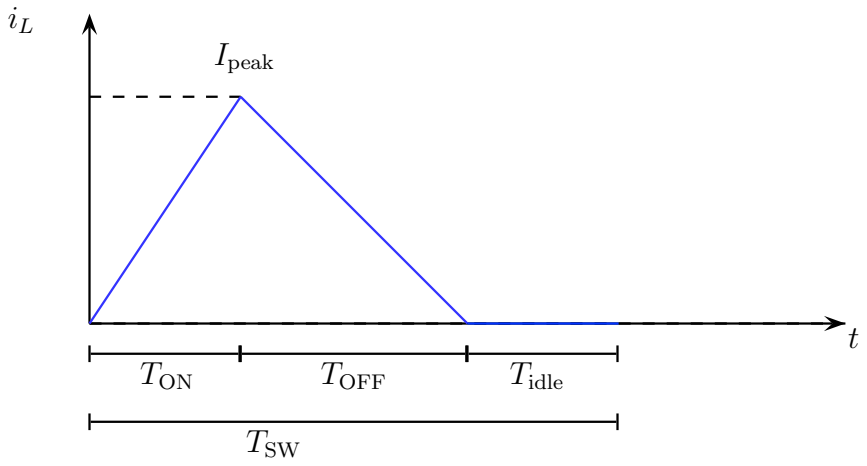
1.4.2 DCM analysis

Before starting with DCM analysis, we want to show something new: when the switch is closed and the diode is open (or during the opposite situation) in a buck converter or in a boost converter we create a direct connection between input and output, passing through the inductor.

In buck-boost converter we can distinguish two specific phases: one, which charges the inductance, and another, which discharges it. This converter is classified as **indirect converter**, because there is not a phase when energy goes directly from the input to the output:



Now, after this introduction, let's start with the DCM analysis:



We have the usual extra time T_3 (the idle time).

We can use the same analysis of all times, calculate the currents on the switch and on the diode, so the currents on the input and output capacitors, and so on; RMS values can be calculated with the sort-of-KCL (or by hand: the *KCL* is theoretically correct, but we have cancellations errors!).

Now, we want to find M for DCM, but we are going to do something new: we have said that this is an indirect converter, because there are two different phases, respect to energy. We know that the energy into an inductance L is:

$$E_L = \frac{1}{2} L I^2$$

The energy we transfer at each cycle is equal to:

$$E_L = \frac{1}{2} L I_{\text{max}}^2$$

in fact, we are not interested on how much time we need to fill the *bucket*, so the inductance: we are just interested in the energy it has!

We already know the expression of I_{max}: we know that I_{min} now equals zero, so we can just use the information about the upper slope:

$$I_{\text{max}} = \frac{V_{\text{in}}}{L} T_1 = \frac{V_{\text{in}}}{L} \frac{D}{f_{\text{SW}}}$$

so:

$$E_{\text{T,cycle}} = \frac{1}{2} L \left(\frac{V_{\text{in}}}{L} \frac{D}{f_{\text{SW}}} \right)^2 =$$

$$= \frac{1}{2} \frac{V_{\text{in}}^2 D^2}{L f_{\text{SW}}^2}$$

This expression is very counter intuitive: E, so the energy transferred, is inversely proportional to L: we reduce the bucket volume, we increase the energy!

We have that the input power equals the energy transferred per cycle, times the switching frequency: switching frequency represents the number of cycles per time!

$$P_{\text{in}} = E_{\text{T,cycle}} f_{\text{SW}}$$

so:

$$P_{\text{in}} = \frac{1}{2} \frac{V_{\text{in}}^2 D^2}{L f_{\text{SW}}} = P_{\text{out}}$$

in fact, for hypothesis, we are assuming no power losses! But we know that:

$$P_{\text{out}} = \frac{V_0^2}{R}$$

so, we can write, just using energy properties, that:

$$\frac{V_{\text{in}}^2 D^2}{2 L f_{\text{SW}}} = \frac{V_0^2}{R}$$

but we want to find M; we can easily invert this expression, and obtain:

$$V_0 = -V_{\text{in}} D \sqrt{\frac{R}{2 f_{\text{SW}} L}}$$

we have to take, of the two solutions of the equation, the **negative** one, because we are using a buck-boost converter, which is an inverting converter!

Now, a couple of observations: if we calculate the usual three parameters, we have:

$$\left. \frac{\partial V_0}{\partial V_{\text{in}}} \right|_{D=\text{constant}} = M_{\text{DCM}}$$

like all times;

$$\frac{\partial V_0}{\partial D} = -V_{\text{in}} \sqrt{\frac{R}{2 f_{\text{SW}} L}} = \frac{V_0}{D}$$

This is not bad: if we don't change our load, if we don't change D, we have that output voltage is proportional to D: we have an almost linear system! But we have something bad: it depends on the load! If we disconnect the

load, we have that $V_0 \to \infty$ (because $M \to \infty$, and this is very bad! We have to take care of the load, to keep it connected for each time, even in closed-loop!

What about the output resistance?

$$\frac{\partial V_0}{\partial I_0} = ...$$

Well, we have to find V_0 as function of I_0:

$$V_0 = -V_{\text{in}} D \sqrt{\frac{\frac{V_0}{I_0}}{2Lf_{\text{SW}}}}$$

so, squaring all the terms:

$$V_0^2 = D^2 V_{\text{in}}^2 \frac{V_0}{I_0} \frac{1}{2Lf_{\text{SW}}}$$

inverting:

$$V_0 = \frac{D^2 V_{\text{in}}^2}{2I_0 f_{\text{SW}} L}$$

so, let's differentiate it:

$$\frac{\partial V_0}{\partial I_0} = \frac{0 - 2D^2 V_{\text{in}}^2 L f_{\text{SW}}}{(2Lf_{\text{SW}} I_0)^2} = -\frac{D^2 V_{\text{in}}^2}{2Lf_{\text{SW}} I_0^2}$$

This is our output resistance; can we write it in a simpler way? Well, remembering that:

$$V_0^2 = V_{\text{in}}^2 \frac{D^2 R}{2f_{\text{SW}} L}$$

we can see that:

$$V_{\text{in}}^2 \frac{D^2 R}{2f_{\text{SW}} L V_0^2} = 1$$

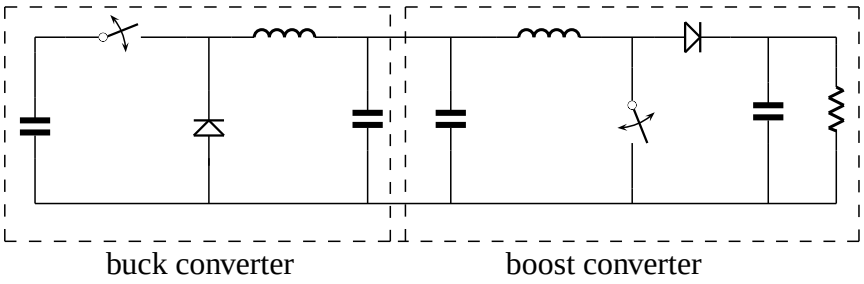
so:

$$\frac{V_0^2}{R} \frac{R^2}{V_0^2} = -R$$

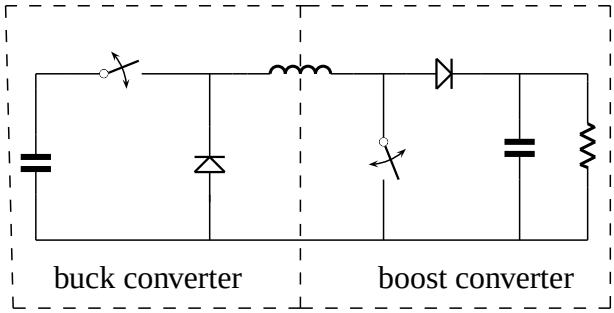
this is not an actual negative resistance: we made our calculations referring just to V_0, without considering that it is referred to the input: actually we have a positive resistance, which equals the load impedance!

1.5 Some notes about basic topologies

We have studied the two basic topologies; now, let's consider how to put them together, and obtain a buck-boost converter (in order to see that it is actually the union of a buck and a boost!); let's consider something like this:



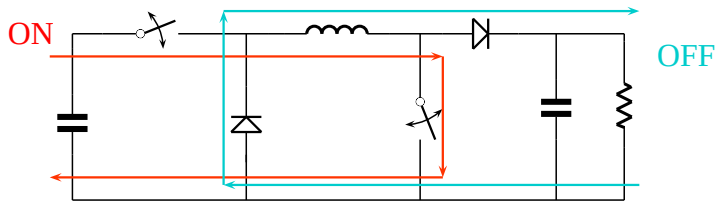
In the center of the schematic we have two capacitors in parallel; the basic idea is to add them, but we can also remove them! They are not important, because they are just a way to improve the output (for buck) and input (for boost) filtering (input capacitor for buck and output capacitor for boost **must not be removed**). So, we can remove those capacitances, and we obtain two inductors in series; by adding them:



$$V_0 = V_{\text{in}} D \frac{1}{1-D}$$

we just multiply the two transfer functions and obtain, except for a negative sign, the buck-boost transfer function: this is a **not-inverting buck-boost**. We can use four switches instead than two switches and two diodes, solution used often for low power integrated converters. Like in the inverting schematic, we have two stressed capacitors.

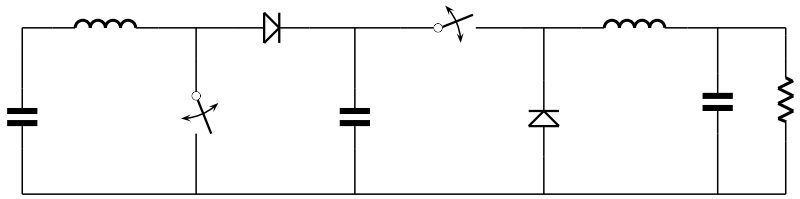
How can we relate this schematic to the previous one? Well, let's consider the two phases:



this inductor for both phases is grounded, but at each cycle we change the ground pin: in the previous (inverting) schematic, we had the same ground pin for the two cycles; now, we are taking the inductor, and flipping it. This can be done, because it is an **indirect** converter: we are still transferring energy one time from input to the inductor, one time from the inductor to the output.

1.5.1 A short introduction to Čuk converters

Professor Čuk realized that this topology is composed of a buck, followed by a boost; his idea was to invent a new topology, the **boost-buck** converter, called Čuk converter:



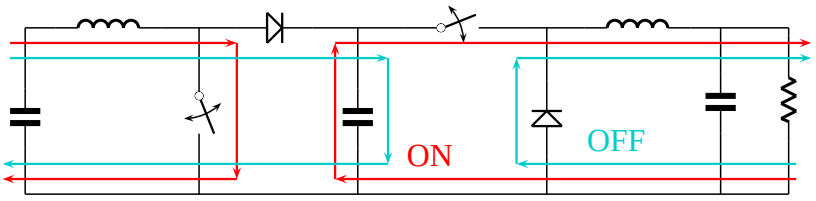
this is dual respect to the previous one.

Input and output capacitor are near to an inductor, so they are not stressed anymore; its gain is:

$$\frac{V_0}{V_{\text{in}}} = \frac{D}{1-D}$$

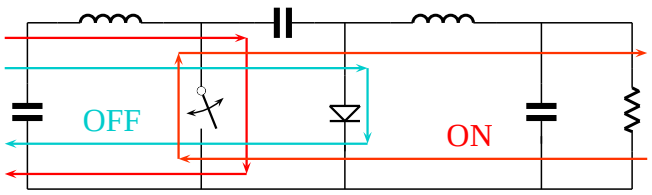
Output voltage can be higher or lower than the output voltage. It is a good converter, but has a big issue: it is **complicated**: it has too components!

If the switches are driven at the same time, together, we have something like this:



During T_1, during the ON phase we close the switches, and we have that the input side is just charging the inductance, and output side taking current out of the capacitor; during the OFF phase, we open the switches, so the boost converter is charging the capacitor, and the buck converter is working with the energy stored in the inductor and in the output capacitor. Energy now is stored in the capacitor: we first charge the capacitor with the boost, disconnect it and connect it to the buck. This capacitor has all the time one pin connected to the ground.

We can change this circuit in this one:



I can flip the capacitor: during T_{ON} the switch is closed, so the left side of the capacitor is grounded, and it is discharging its energy; during T_{OFF}, the switch is open, and the input current flows through the capacitor, charging it. This time we are flipping the capacitor (instead of inductor, like in buck-boost); now, the output voltage equals:

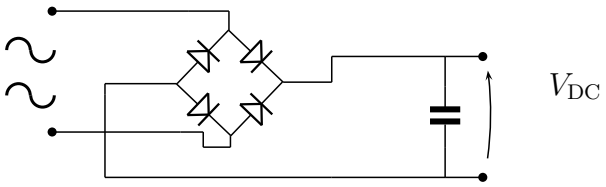
$$V_0 = -\frac{V_{\text{in}} D}{1 - D}$$

this, because now we are also flipping the capacitor.

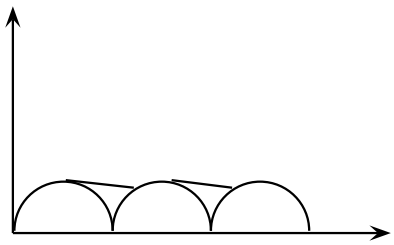
The two inductors can be at the same core, so this can provide simplifications and high performances.

1.6 Off-line rectifiers

Now, we are going to introduce some ideas about rectifications, so about AC/DC conversion: basically, if we want to rectify an AC voltage, we have to do something like this:



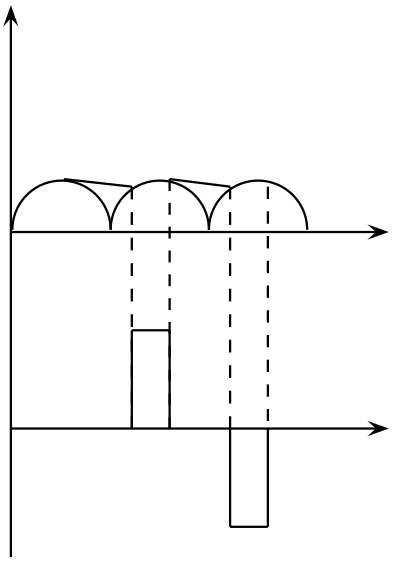
From the input AC, we have to put some diode bridge (like a Graetz bridge), then a low-pass filter, which can be a capacitor: the source of this voltage filter will be a non-linear source: as usual, a low-pass filter returns an average, a DC voltage: if we have a linear source like a resistor, the voltage across the capacitor is the average value of the voltage on it; now, the source is non-linear, so, in this case, instead of the average, we have the peak value (with some losses):



Actually, this is not a DC voltage: we have some ripple, which can be reduced simply by increasing the capacitor value.

This rectifier has a large inrush current: we have to charge the (big) capacitor, and, if we stop the switch, the derivative of voltage respect to time increases: inrush current is so very high.

Now: when diodes are conducting? Well: they, after the transient, are conducting just when we reach the sine: if we want to remember what the previous plot says, is: after the transient, we have an output voltage, which is basically equal to the peak of the rectified waveform; when the rectified sine begins to come down, the DC voltage, due to losses or something similar, begins to decrease, until reaches the value of the rectified voltage (which comes up, after a certain time); for a little time, diodes are conducting, in order to charge the capacitor, in order to fill it and making its output voltage equal to the ideal V_{DC}. The current of the diodes, which is the current taken from the input source, is a pulsating current:



Current is taken just from narrow pulses. This brings two great issues:

- it generates a lot of noise;
- it is very bad for the power company, because of a complicated reason we are going to show soon; an idea is: if there are many non-linear loads which take the current like this, we have a pulsating waveform.

  We have that there is an almost waveform, with some peaks.

Let's focus on the second point: this pulsating current is periodic, so we can expand it with Fourier series:

$$i(t) = \sum_{n=1}^{\infty} a_n \sin(n\omega t + \varphi_n)$$

those peaks are symmetrical, so the $i(t)$ function is odd respect to time; this means that Fourier expansion will have just odd terms (sine terms). We know that:

$$v(t) = V_{\text{pk}} \sin(\omega t)$$

where ω is the pulsation of the input voltage.
Now, we can find the power just saying that:

$$p(t) = v(t)i(t)$$

We have no power for most of the time, and then very high power pulses; this is interesting, but we can do something more: we can calculate average power!

$$\overline{p(t)} = \overline{v(t)i(t)} = \overline{V_{\text{pk}} \sin(\omega t) \sum_{n=1}^{\infty} a_n \sin(n\omega t + \varphi_n)}$$

There are common sense rules and laws about n: we wrote ∞, but usual $n = 4$ is a good limit.

Now, let's calculate this average using math: for a generic n-th term, we have something like:

$$\frac{1}{T} \int_0^T V_{\text{pk}} a_n \sin(\omega t) \sin(n\omega t) \mathrm{d}t$$

This is the average contribute for a generic term of the sum, so for the n-th harmonic of the spectrum. Now, an observation: Fourier series is an orthogonal base of L^2, so, respect to another sinusoidal waveform, it is orthogonal: if we calculate the integral, in a period, of the product of two harmonics, if the harmonics are the same, the integral is different from zero; in other cases, it is zero.

About the first harmonic:

$$\frac{1}{T} \int_0^T V_{\text{pk}} a_1 \sin(\omega t) \sin(\omega t) \mathrm{d}t = \frac{V_{\text{pk}}}{2} a_1 \cos(\varphi_1)$$

About the other harmonics, they don't bring contributes into the average power.

What happens in practice? Well, if we have a 50 Hz main harmonic, remembering that the second one does not exists, the third one, 150 Hz, don't bring any contribute to the load (which receives only the fundamental one, due to the filtering, as already seen), but dissipates all its contribute through the wire! Power companies are not happy about this type of harmonic dissipation, because they inject *high* (actually no so high!) frequency harmonics in the network, dissipating power, so they introduced very strict rules about the use/non-use of the pulsing current.

Unless some cases, we are **not allowed** to absorb current like this.

If we can't use these rectifiers, what can we do? Well, the part which makes the current be pulsating is the diode bridge with the capacitor; we **need** this bridge, because we have to rectify the input waveform in some way, but we have to avoid the capacitor, because it is charged with that pulsating waveform.

Our rectifier must be something which is not a capacitor, but it is a problem: this makes current not be a constant, but something variable! There is no way to obtain it! An idea is to have something which looks like a resistance: with this kind of load, current will be just attenuated, but sinusoidal, in phase with the input voltage.

So: what companies want to see is a resistive load, so something which has an output current in phase with the input voltage, sinusoidal; what we want is a DC output voltage: this is the problem of realizing a PFC.

A PFC (Power Factor Corrector) is something which seems a resistor for the company, and a DC delivery circuit for us.

What is the power factor? Well, let's see: the average of the power of two signals is:

$$\overline{v(t)i(t)} = \frac{V_{\text{pk}} I_{\text{pk}}}{2} \cos(\varphi)$$

this is the average power. Let's remark that I_{pk} is relative to the **fundamental** (as seen just before), and φ is the phase between input voltage and output first harmonic current.

The **active** power can be written as:

$$P_{\text{active}} = V_{\text{RMS}} I_{\text{RMS}}$$

but, if our load is not resistive, we have that this $\cos(\varphi)$ is different than 1; we obtain two variations:

$$P_{\text{active}} = V_{\text{RMS}} I_{\text{RMS}} \cos(\varphi) F_{\text{D}}$$

The first one is just the introduction of the well-known cosine; the second one is this: an RMS value is evaluated using **all harmonics** in the waveform; what we are using is not the whole RMS, but just the fundamental component! This F_{D}, called **distorsion factor**, is defined as:

$$F_{\text{D}} = \frac{I_1}{I_{\text{RMS}}}$$

where I_1 is the first harmonic of the output current (in Europe, 50 Hz, in USA, 60 Hz). F_{D} is just the ratio of the two quantities. The power factor is defined as:

$$F_{\text{P}} = \cos(\varphi) \frac{I_1}{I_{\text{RMS}}}$$

This is the actual definition of power factor; previously all the engineers used just the first term, because most of the loads were motors, and motors have both inductive and resistive parts; now our loads are electronics,

so the distorsion part is very important. The cosine term, now, is called **displacement factor**.

1.6.1 PFC with switching converters

Now, how can we realize this PFC ? Well, first of all, we need a constant voltage out of our system: a DC. A way to do it is to put a huge low-pass filter, which filters all the harmonics, but it is impossible: too expensive and large.

Instead to do this, we can use electronics: we can transform this voltage into an output voltage, which is almost constant. Now: which circuit can we use, to do it?

First idea can be: let's use a buck! Can we? Well, a buck is a step-down converter, so we have to put the output voltage at a certain level.

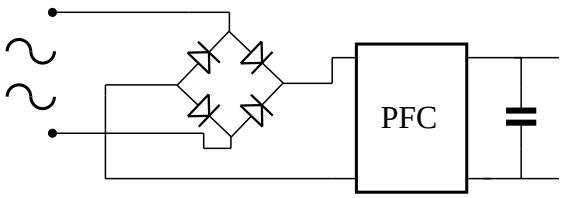
Surely we can step-down the higher voltage values, but there's no way to step up some values! What we obtain is a crosstalk distorsion: some silent intervals!

The good idea is to use a boost converter: if I place the voltage over all the waveform, every value can be raised. It works! Every value can be raised to the point! The critical points are the lowest ones, because we need larger boost factor, but we have seen that the boost factor increases until it changes slope, falling down; this is a bad news, but the saturation point for the boost factor is related to losses, to parasitic resistances: currents will be low, so we can do it! There is another intrinsic advantage: at the input, we have a low-pass filter, which removes noise! Another advantage: it can be used to realize **universal** power supplies, because we just have to put the output voltage on a point higher than the peak value of all the world; this can be a little critical for Australia (which has 240 V_{RMS} in the line), but, for these cases, we can step down with a first stage (which generally is not a buck), and then use the boost PFC.

A note: we have to isolate this topology: after the PFC we need a second stage, which must be isolated, in order to decouple the references and prevent risks of many types for the user and for the electronics.

What about buck-boost as PFC? Well, in this case, the polarity is opposite, so we can use it as PFC. It works, but it can be a bad idea to use small output voltages (we want to have large M, in order to make the buck-boost work well), so good voltages can be -50 V or -100 V. These converters are not many used because they have a pulsating input current, so we have to put a large EMI filter, which is very expensive: it is better to have a boost converter.

Previously, we used the energy approach to do the analysis: this can be also used in a PFC, with an input voltage, a certain input current, and on the output we will get this:



Which is the instantaneous input power? Well:

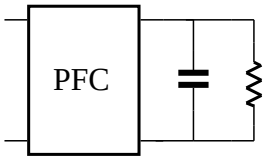
$$p(t) = v(t)i(t)$$

The frequency of this wave is the double of the input wave frequency, and:

$$P_{\text{AVE}} = \frac{1}{2}P_{\text{pk}}$$

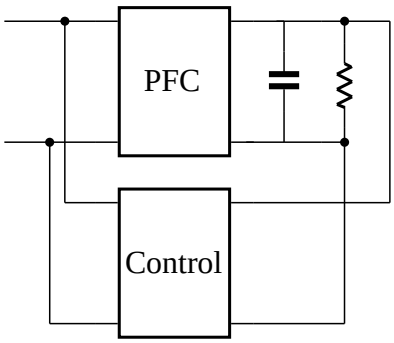
this, for the properties of the sine with the powers.

What about the output voltage? Well, we want to use something like this:



This load, in order to provide a DC, must have a constant output power: we have to provide some extra power, and an energy storage which can store for 5 ms, and release it for other 5 ms: we need something which maintains constant the output power. Our luck is that the average value of the input power, which is the desired output power, is half of the waveform, so basically it is an energy storage! When the load has too much power, this is taken by the output capacitor in order to don't send it to the load; when the load is less driven, the capacitor gives power to the load.

A little issue: when we store and remove current through the capacitor, we have current flow on it, and so voltage changes: we don't have an actual DC voltage, but something similar: voltage will increase and decrease like this:



This ripple isn't easy to control.
Now:

$$\frac{1}{2}CV_1^2 - \frac{1}{2}CV_2^2 = \Delta E$$

So, thanks to the relations previously explained, we have that the energy change is related to the voltage change, so to the ripple!

Now, the capacitor value is very important: we are at 100 Hz, so we have to control it: at these frequencies, capacitor behaves as a capacitance, so we have to care also about it!

Why boost can be used for PFC? Well, we said that a boost converter is hard to control, because it has a zero at the right half-plane.

The control circuit takes a sample of the input and output voltages, combine them, produce an error signal and drive the circuit. Can we maintain a quite constant output voltage? Well, if we want to have a DC, without ripples, the output voltage is totally constant, and so also the output power: we are delivering a constant power to the load. If we remove the output ripple, this means that the input power is constant too, but we also know that v_{in} must be a sinusoidal waveform; what happens is that:

$$i_{\text{in}} = \frac{P_{\text{in}}}{v_{\text{in}}}$$

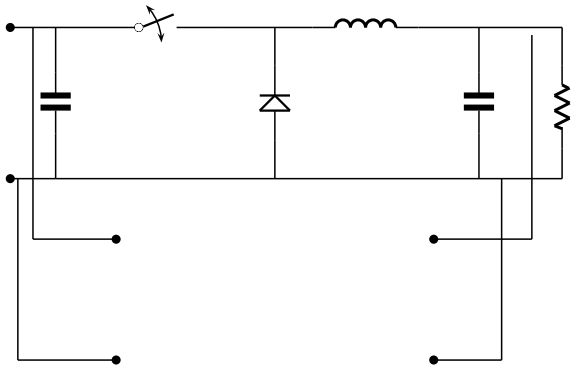
where P_{in} is constant, and v_{in} has two zeroes for each period: the input current **is not a sine**! This means that we **have to** store and release energy, because, if we don't, the PFC does not behaves as we want.

How may I design a control circuit which is blind respect to the 100 Hz ripple? We need it, because it is physiological, good: in order to do it, it must be blind to the frequency of that ripple, so we can close the loop with a low pass filter before the control, with a frequency very lower respect to 100 Hz; a good idea can be to use something like 10 Hz. This introduces another positive fact: the right-zero of the boost is at a higher frequency respect to

the 10 Hz of the filter we already introduced: this means that we don't have to care about it any longer!

End of the chapter

We want now to end this chapter, by introducing the following one; let's consider one of our circuits (for example, the buck converter):



Output voltage must be constant; what we have to do, so, is to measure with some circuit the output, and control it by changing something (for example D): we have to close the loop, introduce a feedback, and so we may have some instabilities. There is a problem: the circuits we analyzed are:

- time-variant (each time the switch changes its position, the topology of the circuit changes!);
- non-linear : there are non-linear elements, such as the switch or the diode.

This is very bad. Out next purpose will be to *average* our circuit, and obtain a time-invariant non-linear circuit; we will linearise it, and then obtain an LTI circuit, easier to control.

Chapter 2

Modelling of switching-mode converters

Now we are going to work to the modelling of our converter: find the relations between duty cycle and output voltage, but in the Laplace domain, in order to obtain a transfer function, from whom we can design the feedback control system. What we need is something like:

$$h(s) = \frac{v_0(s)}{d(s)}$$

What do we have and what do we need? Well, if we want to use the formalism of transfer functions, we need a linear system: starting from the actual time-variant non-linear system we have to **average** it and obtain a time-invariant non-liner system, which can be linearized, in order to obtain an LTI system. There are many different methods for averaging a circuit: in order to do it, we have to average a quantity $x(t)$, for example by taking this integral:

$$\overline{x(t)} = \frac{1}{T_{\mathrm{SW}}} \int_t^{t+T_{\mathrm{SW}}} x(\tau)\mathrm{d}\tau$$

this, supposing (it is not mandatory) that our quantity $x(t)$ is periodic of T_{SW}. This kind of average is known as **moving average**: if we move the average of a periodic signal, and T_{SW} is the period of this signal, we have a **constant value**. Another possible way to average something is this:

$$x(n) = \frac{1}{T_{\mathrm{SW}}} \int_{nT_{\mathrm{SW}}}^{(n+1)T_{\mathrm{SW}}} x(t)\mathrm{d}t$$

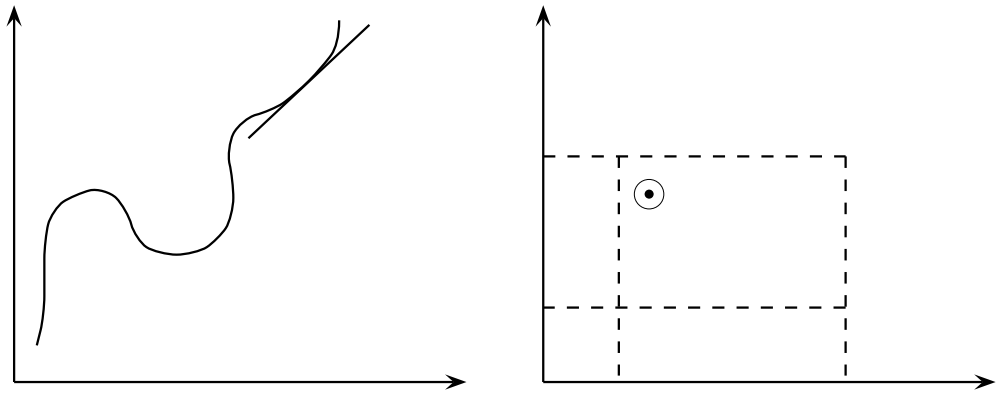
this is a **discrete average**: from the first average method we had a single

value; now, we have a **sequence of numbers**, which can be processed using $\mathcal{Z}$ transform and so on.

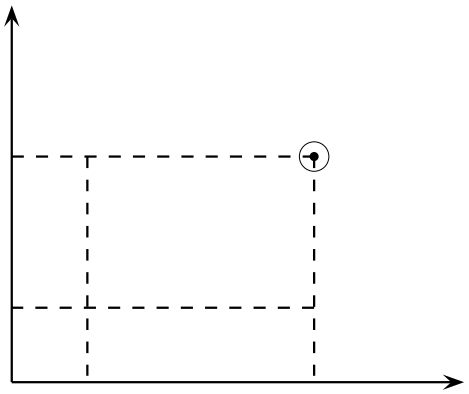
From the first average in general we obtain a **function**; with the second, a **sequence of numbers**. Which advantages/disadvantages do we have from these processes? Well, in both cases we lose the behaviour hidden inside one cycle: we don't know anything about the shape of the signal, peak values, $I_{\max}$, $I_{\min}$, I_{RMS}: everything is reduced to one single number. From the second average we have something similar, but we can see it better in the frequency domain: the second operation is similar to a sampling process: we *average* f_{SW} times per second. The sampling theorem says that we have to sample at the double of the frequency of the system; what we have now is that our analysis will be valid, limited, up to half of f_{SW}: our models stop to be valid at $\frac{f_{\text{SW}}}{2}$.

Which are the advantages? Well, at these levels, we have a **time-invariant** circuit: this is easy to handle, even for simulators like SPICE! Every time we have to handle with SPICE a time-variant circuit (something with switches or something else) we need a very very long simulation time: with similar circuits, but time-invariant, the time decreases of one or two orders of magnitude (for example, one hour to one second).

Once we have a time-variant system, linearize it is simple: we can use the Taylor expansion theory, and cut up to the first term: this means that, with this last operation, we lose the large signal behaviour: of all the non-linear behaviour of the system we take just the slope of the tangent line in a certain point: the approximation we take from the small-signal model is just a local information:



we have informations just for a little region around the linearization point. There are infinite values we can use to perform the linearization (around whom linearize the system), but a good idea can be to use the critical ones (like the corners): by this way, using critical point, when we design the control we may lose some performances, but obtain stability everywhere!

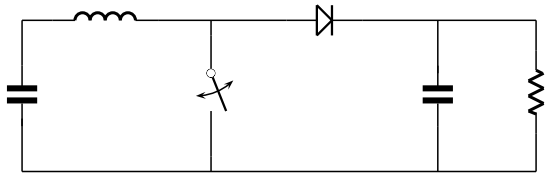


Our control system will be quite easy: an opamp and some passive components (such as capacitors and resistors).

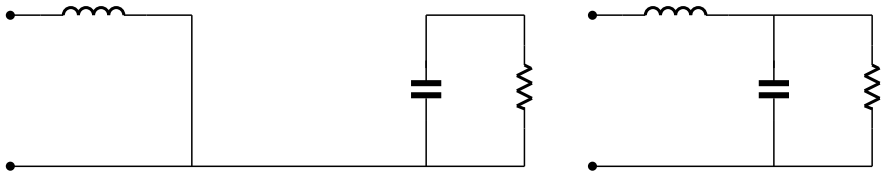
2.1 State space averaging

We are going to analyze a technique which works in every situation, but which has a lot of calculations (easy calculations, high-school algebra!), which must be solved in a quite mechanical way.

The basic idea of this technique is: let's take a circuit, for example the boost circuit in CCM:



we have that its switch keeps opening and closing all time long; when the switch is fixed in its position, we have two different topologies: one during T_{ON}, one during T_{OFF}:



let's consider with 1 the topology with the closed switch, and with 2 the topology with the open switch.

Now: let's forget that these two circuits derive from a switch-mode power converter: now, they are just two LTI circuits, so circuits which can be

studied with the formalism of differential equations! Unfortunately, we have that these circuits last for a short time, but, just for the single times T_{ON} and T_{OFF}, we can write down the differential equations for them. In a general way, we can write that, for a LTI system.

$$\dot{\mathbf{x}} = \mathbf{A}\mathbf{x} + \mathbf{B}\mathbf{u}$$

where $\dot{\mathbf{x}}$ is the time derivative of $\mathbf{x}$, which is the **state vector** (so the vector of the state variables of the system), $\mathbf{u}$ the **input vector** (so the vector of the inputs of the system), and the matrices are what characterize each system: the two circuits will differ for $\mathbf{A}$ and $\mathbf{B}$. Usually there are also other two matrices, which we will ignore, because, in this case, the output is a state variable.

Let's define the two vectors of the problem:

$$\mathbf{x} = \begin{bmatrix} i_L \\ v_0 \end{bmatrix}$$

The actual state variable is v_{C_0}, but it equals the output voltage. What about $\mathbf{u}$? Well, it is scalar, because we can consider just v_{in} as input of our system; be careful: another input is i_0, because we have to consider as input **everything which changes the bias point**; we know the relation between i_0 and the state variable v_0 (because there is a relation thanks to the load resistance R), so the input vector will be just the input voltage.

A remark about initial and final conditions: the final value for T_{ON} is the initial value T_{OFF}, and *vice versa*: with these conditions we can solve those differential equations.

Let's identify the two matrices for the two circuits:

1. for the first circuit:

$$\begin{cases} L\frac{\mathrm{d}i_L}{\mathrm{d}t} = v_{\mathrm{in}} \\ C_0\frac{\mathrm{d}v_0}{\mathrm{d}t} = -\frac{v_0}{R} \end{cases}$$

by cleaning (considering just the derivatives at the left member, and defining $C \triangleq C_0$):

$$\begin{cases} \frac{\mathrm{d}i_L}{\mathrm{d}t} = \frac{v_{\mathrm{in}}}{L} \\ \frac{\mathrm{d}v_0}{\mathrm{d}t} = -\frac{v_0}{RC} \end{cases}$$

so, using the matrix formalism, we have:

$$\dot{\mathbf{x}} = \mathbf{A}_1\mathbf{x} + \mathbf{B}_1\mathbf{u}$$

this becomes (by inspection):

$$\dot{\mathbf{x}} = \begin{bmatrix} 0 & 0 \\ 0 & -\frac{1}{RC} \end{bmatrix} \begin{bmatrix} i_L \\ v_0 \end{bmatrix} + \begin{bmatrix} \frac{1}{L} \\ 0 \end{bmatrix} v_{\text{in}}$$

2. for the second circuit:

$$\begin{cases} L\frac{\mathrm{d}i_L}{\mathrm{d}t} = v_{\text{in}} - v_0 \\ C_0\frac{\mathrm{d}v_0}{\mathrm{d}t} = i_L - \frac{v_0}{R} \end{cases}$$

by cleaning (considering just the derivatives at the left member, and defining $C \triangleq C_0$):

$$\begin{cases} \frac{\mathrm{d}i_L}{\mathrm{d}t} = \frac{v_{\text{in}} - v_0}{L} \\ \frac{\mathrm{d}v_0}{\mathrm{d}t} = \frac{i_L}{C} - \frac{v_0}{RC} \end{cases}$$

so, using the matrix formalism, we have:

$$\dot{\mathbf{x}} = \mathbf{A}_2\mathbf{x} + \mathbf{B}_2\mathbf{u}$$

this becomes (by inspection):

$$\dot{\mathbf{x}} = \begin{bmatrix} 0 & -\frac{1}{L} \\ \frac{1}{C} & -\frac{1}{RC} \end{bmatrix} \begin{bmatrix} i_L \\ v_0 \end{bmatrix} + \begin{bmatrix} \frac{1}{L} \\ 0 \end{bmatrix} v_{\text{in}}$$

Now, with an ODE solver, we can put these matrices and solve the system. Problem: we don't are ODE solvers! We want something different!

What we can do now is: let's work with just the **weighted average** of the two matrices, merging them into one single matrix, and this will be our average system; instead of $\mathbf{A}_1$ and $\mathbf{A}_2$, we will have:

$$\mathbf{A} = \mathbf{A}_1\mathbf{d} + \mathbf{A}_2(\mathcal{I} - \mathbf{d})$$

where $\mathbf{d}$ is the vector of duty cycles, $\mathcal{I}$ the identical matrix (or, this time, the identical vector).

This method has some reasonable probability to work.

Scalar example

In order to understand why what we have done has some sense, let's consider a simplified example, with just one dimension:

- during T_{ON},

$$\dot{x} = a_1 x$$

- during T_{OFF},

$$\dot{x} = a_2 x$$

Which is the evolution of this system, in time domain? Well, from Calculus 1, we know that the solution of these expressions are exponentials:

$$x(t) = \mathrm{e}^{-a_1 t} x(0)$$

This system, like the former one, switches every time from one to the other equation. We have to find the final condition, so the value of x in the time T_{ON}:

$$x(T_{\mathrm{ON}}) = \mathrm{e}^{-a_1 T_{\mathrm{ON}}} x(0)$$

this is what happens, in the first system, after T_{ON}. Well, we know that the second equation is something like this (considering also the time shift):

$$x(t + T_{\mathrm{ON}}) = \mathrm{e}^{-a_2 t} x(T_{\mathrm{ON}})$$

of this system we are interested to find the final condition (like we've done in the previous case); the final condition, in the instant T_{SW}, equals $t = T_{\mathrm{OFF}}$: in fact, we have t shifted by T_{ON}, and $t = T_{\mathrm{OFF}}$, the argument of the function will be T_{SW}:

$$x(T_{\mathrm{OFF}} + T_{\mathrm{ON}}) = x(T_{\mathrm{SW}}) = \mathrm{e}^{-a_2 T_{\mathrm{OFF}}} x(T_{\mathrm{ON}})$$

now, let's remember the previous final condition, and substitute into the second equation:

$$x(T_{\mathrm{SW}}) = \mathrm{e}^{-a_2 T_{\mathrm{OFF}}} \mathrm{e}^{-a_1 T_{\mathrm{ON}}} x(0)$$

With this trick we have just one differential equation:

$$x(T_{\mathrm{SW}}) = \mathrm{e}^{-(a_1 T_{\mathrm{ON}} + a_2 T_{\mathrm{OFF}})} x(0)$$

let's introduce T_{SW} into the equation: in order to do it, we multiply and divide the exponent for T_{SW}, obtaining:

$$x(T_{\mathrm{SW}}) = \mathrm{e}^{-(a_1 T_{\mathrm{ON}} + a_2 T_{\mathrm{OFF}}) \frac{T_{\mathrm{SW}}}{T_{\mathrm{SW}}}} x(0) =$$

$$= \mathrm{e}^{-(a_1 D + a_2 (1-D)) T_{\mathrm{SW}}} x(0)$$

We have, now, an equivalent time constant equal to:

$$a = a_1 D + a_2 (1 - D)$$

this is very similar to what we have done, but with the matrices!

Get back to matrices

Let's continue with matrices: also with them, we want an **average time constant**:

$$\mathbf{A} = \mathbf{A}_1 \mathbf{d} + \mathbf{A}_2 (\mathcal{I} - \mathbf{d})$$

Using simple matrix algebra, we can easily obtain:

$$\mathbf{A} = \begin{bmatrix} 0 & -\frac{1-D}{L} \\ +\frac{1-D}{C} & -\frac{1}{RC} \end{bmatrix} \qquad \mathbf{B} = \begin{bmatrix} \frac{1}{L} \\ 0 \end{bmatrix}$$

Very bad news: this $\mathbf{A}$ is the matrix which represents the behaviour of the averaged system, and its eigenvalues are related to the pole positions of the system; these eigenvalues are depending on the duty cycle D: if we change the bias point, our poles **move**. This system is not linear (as we will see better later): D changes in time, so we are talking about poles, but this is wrong: non-linear systems cannot be described in terms of poles or zeroes, because this formalism belongs to the transfer function formalism, and it can be applied just on linear systems.

This is not the worst news: all this stuff is mathematically wrong! The previous example, where we used all our tricks, was scalar: with matrices, we have that:

$$\mathrm{e}^{\mathbf{A}} \mathrm{e}^{\mathbf{B}} \neq \mathrm{e}^{\mathbf{A}+\mathbf{B}}$$

in fact, we have that:

$$\mathrm{e}^{\mathbf{A}} = \mathbf{A}_1$$

$$e^{\mathbf{B}} = \mathbf{A}_2$$

and this product is not commutative:

$$\mathbf{A}_1\mathbf{A}_2 \neq \mathbf{A}_2\mathbf{A}_1$$

this is **mandatory**, in order to have the exponential of the sum: sum is a commutative operator also with matrices, so the two operations are incompatible.

How can we fix our theory? Well, the exponential of the matrix can be evaluated, using Taylor expansion, as:

$$e^{\mathbf{A}} \sim \mathcal{I} + \mathbf{A} + \frac{\mathbf{A}^2}{2} + ...$$

We have to evaluate this product:

$$e^{\mathbf{A}_1 T_{\text{ON}}} e^{\mathbf{A}_2 T_{\text{OFF}}}$$

this product, as we have just said, is non-commutative; we can introduce some more hypothesis: all the times we have supposed that the time constants are far higher than the switching period T_{SW}; if this is true, we have that the time constant for the matrices are far larger than T_{ON} and T_{OFF}, so, when we are evaluating $\mathbf{A}_1 T_{\text{ON}}$ and $\mathbf{A}_2 T_{\text{OFF}}$, we have *small matrices*, in a wide sense (we can evaluate this by finding the norms of the matrices in some sense and verify this idea). What we can do, so, is use the Taylor expansion up to the first term, and neglect all the other terms!

$$e^{\mathbf{A}_1} \sim \mathcal{I} + \mathbf{A}_1 T_{\text{ON}}$$

$$e^{\mathbf{A}_2} \sim \mathcal{I} + \mathbf{A}_2 T_{\text{OFF}}$$

so:

$$(\mathcal{I} + \mathbf{A}_1 T_{\text{ON}})(\mathcal{I} + \mathbf{A}_2 T_{\text{OFF}}) = \mathcal{I} + \mathbf{A}_1 T_{\text{ON}} + \mathbf{A}_2 T_{\text{OFF}} + \mathbf{A}_1\mathbf{A}_2 T_{\text{ON}} T_{\text{OFF}}$$

but there is a second order term, related to the product of the two matrices! From one side, it makes our system be non-commutative; from the other side, it is a second order term, so it is smaller than the others, and can be neglected! So:

$$e^{\mathbf{A}_1 T_{\text{ON}}} e^{\mathbf{A}_2 T_{\text{OFF}}} \sim \mathcal{I} + \mathbf{A}_1 T_{\text{ON}} + \mathbf{A}_2 T_{\text{OFF}}$$

This is commutative, so, given our hypothesis, this derivation is right.

Our system, now, is described by this differential equation:

$$\dot{\mathbf{x}} = \mathbf{A}\mathbf{x} + \mathbf{B}\mathbf{u}$$

The variables of this system are: i_L, v_0, $\hat{v}_{\text{in}}$, d (the duty cycle). Let's write the system as two parts: steady state (constant values) and small signal:

$$i_L = I_L + \hat{i_l}$$

$$v_0 = V_0 + \hat{v_0}$$

$$\hat{v}_{\text{in}} = V_{\text{IN}} + \hat{v_{\text{in}}}$$

$$d = D + \hat{d}$$

where the *hat* parameters are the variations around the steady state; the capitals variables are the steady-state values.

The two equations, considering steady state and variable terms, are:

$$\frac{\mathrm{d}}{\mathrm{d}t}\left(I_L + \hat{i_l}\right) = -\frac{1 - D - \hat{d}}{L}\left(V_0 + \hat{v_0}\right) + \frac{1}{L}\left(V_{\text{IN}} + \hat{v_{\text{in}}}\right)$$

$$\frac{\mathrm{d}}{\mathrm{d}t}\left(V_0 + \hat{v_0}\right) = \frac{1 - D - \hat{d}}{C}\left(I_L + \hat{i_l}\right) - \frac{V_0 + \hat{v_0}}{RC}$$

These are non-linear differential equations: we have no switches (the system is time-invariant), but there are terms like $\hat{d}\hat{v_0}$, so the product of two variable terms, which introduce non-linearities.

In order to perform the linearization, we can introduce this hypothesis: if the *hat* terms are very less respect to the DC terms, we can neglect the second order terms. We will do it later.

Let's consider these equations, with just the DC terms:

$$\frac{\mathrm{d}}{\mathrm{d}t}I_L = -\frac{1 - D}{L}V_0 + \frac{V_{\text{IN}}}{L}$$

$$\frac{\mathrm{d}}{\mathrm{d}t}V_0 = \frac{1 - D}{C}I_L - \frac{V_0}{RC}$$

so: the derivatives of constant (DC) terms are null, and we can say that:

$$-\frac{1 - D}{L}V_0 + \frac{V_{\text{IN}}}{L} = 0 \longrightarrow (1 - D)V_0 = V_{\text{IN}}$$

and

$$\frac{V_0}{V_{\text{IN}}} = \frac{1}{1-D}$$

but... This is just the DC gain of the boost! It is a check: what we have done is all right!

About the second equation:

$$\frac{1-D}{C} I_L - \frac{V_0}{RC} = 0 \longrightarrow (1-D) I_L = \frac{V_0}{R}$$

so

$$I_L = \frac{V_0}{R(1-D)} = \frac{I_0}{1-D}$$

this transforms the current from right to left, with an inverse relation.

This was just a check; now, let's focus on important results:

$$\frac{\mathrm{d}}{\mathrm{d}t}\hat{i_l} = -\frac{1-D}{L}\hat{v_0} + \frac{\hat{d}}{L}V_0 + \frac{\hat{d}\hat{v_0}}{L} + \frac{\hat{v}_{\text{in}}}{L}$$

$$\frac{\mathrm{d}}{\mathrm{d}t}\hat{v_0} = \frac{1-D}{C}\hat{i_l} - \frac{\hat{d}}{C}I_L - \frac{\hat{d}\hat{i_l}}{C} - \frac{\hat{v_0}}{RC}$$

These are our non-linear signal equations; **if and only if** we are in small signal condition, we can neglect the second order terms; second order conditions are:

$$\begin{cases} D \gg \hat{d} \\ I_L \gg \hat{i_l} \\ V_0 \gg \hat{v_0} \end{cases}$$

So, if we satisfy these conditions, we can linearize our equation, simply by erasing all the terms, re-writing them without the second order terms:

$$\frac{\mathrm{d}}{\mathrm{d}t}\hat{i_l} = -\frac{1-D}{L}\hat{v_0} + \frac{\hat{d}}{L}V_0 + \frac{\hat{v}_{\text{in}}}{L}$$

$$\frac{\mathrm{d}}{\mathrm{d}t}\hat{v_0} = \frac{1-D}{C}\hat{i_l} - \frac{\hat{d}}{C}I_L - \frac{\hat{v_0}}{RC}$$

Now, our purpose is to find the transfer function: let's move to Laplace domain:

$$s\hat{i_l}(s) = -\frac{1-D}{L}\hat{v_0}(s) + \frac{\hat{d}(s)}{L}V_0 + \frac{\hat{v}_{\text{in}}(s)}{L}$$

$$s\hat{v_0}(s) = \frac{1-D}{C}\hat{i_l}(s) - \frac{\hat{d}(s)}{C}I_L - \frac{\hat{v_0}(s)}{RC}$$

Those equation are algebraic and linear! This means that we can use the superposition effect: we have two inputs, but, if we want to find the transfer function between the duty cycle and the output voltage, we just have to **set**

$$\hat{v}_{\text{in}}(s) = 0$$

A remark: this is not neglecting or other: we are using the linearity property, and trying to calculate the transfer function.

Let's derive the expression of $\hat{i_l}(s)$ from the first equation, then substitute it into the second one:

$$\hat{i_l}(s) = -\frac{1-D}{sL}\hat{v_0}(s) + \frac{\hat{d}(s)}{sL}V_0$$

so:

$$s\hat{v_0}(s) = \frac{1-D}{C}\left[-\frac{1-D}{sL}\hat{v_0}(s) + \frac{\hat{d}(s)}{sL}V_0\right] - \frac{\hat{d}(s)}{C}I_L - \frac{\hat{v_0}(s)}{RC}$$

let's clean some terms:

$$\hat{v_0}(s)\left[s + \frac{(D-1)^2}{sLC} + \frac{1}{RC}\right] = \hat{d}(s)\left[\frac{1-D}{C}\frac{V_0}{sL} - \frac{I_L}{C}\right]$$

Now, two observations: as already seen:

$$V_0 = \frac{V_{\text{IN}}}{1-D}$$

$$I_L = \frac{V_0}{R(1-D)} = \frac{V_{\text{IN}}}{R(1-D)^2}$$

We can substitute it, and obtain:

$$\hat{v_0}(s)\left[s + \frac{(D-1)^2}{sLC} + \frac{1}{RC}\right] = \hat{d}(s)\left[\frac{1-D}{C}\frac{V_{\text{IN}}}{sL(1-D)} - \frac{V_{\text{IN}}}{RC(1-D)^2}\right]$$

so, let's bring out V_{IN}, simplify, and multiply both members times sLC:

$$\hat{v_0}(s)\left[s^2LC + (D-1)^2 + \frac{sL}{R}\right] = \hat{d}(s)\left[1 - \frac{sL}{R(1-D)^2}\right]V_{\text{IN}}$$

Finally:

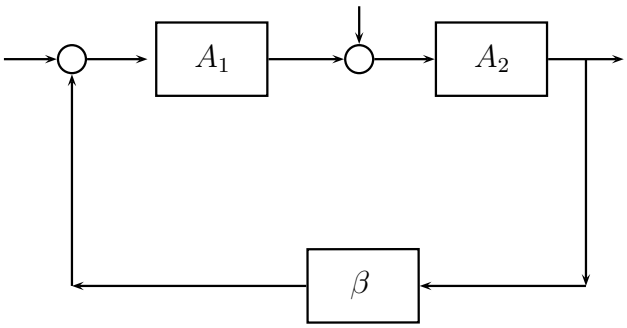
$$\frac{\hat{v_0}}{\hat{d}} = V_{\text{IN}} \frac{1 - s\frac{L}{R(1-D)^2}}{s^2 LC + s\frac{L}{R} + (1-D)^2}$$

let's take out $(1-D)^2$ from the denominator, and obtain the final expression:

$$\frac{\hat{v_0}}{\hat{d}} = \frac{V_{\text{IN}}}{(1-D)^2} \frac{1 - s\frac{L}{R(1-D)^2}}{\frac{s^2 LC}{(1-D)^2} + s\frac{L}{R(1-D)^2} + 1}$$

Now, with this expression, we are able to design our controller; why did we set $\hat{v_{\text{in}}} = 0$? Well, for two reasons:

- why not? This is a linear system!
- Because, when we design our loop gain, we are **not** interested in the input, but in the duty cycle, which is the control parameter!



Now, we have this transfer function, represented as product of DC gain and frequency-dependent part; if we calculate the limit for infinite time:

$$\lim_{s \to 0} \frac{\hat{v_0}}{\hat{d}} = \frac{V_{\text{IN}}}{(1-D)^2}$$

This is what we've found with our former analysis!

The poles are moving, depending on D:

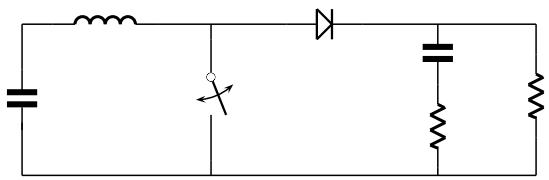
$$f_{\text{P}} = \frac{1-D}{2\pi\sqrt{LC}}$$

so, our frequency limits depend on duty cycle!

Very very bad news: the worst information we get from this transfer function is the negative sign at the numerator: it means that we have a right half-plane zero! Control a system like this is very very hard!

Some additional notes

Now, let's consider a circuit like this one, which considers the presence of an ESR R_{S} on the output capacitor:



With this ESR, at the numerator we have (it can be proof) a second zero, this time on the left half-plane (a good zero!): something like:

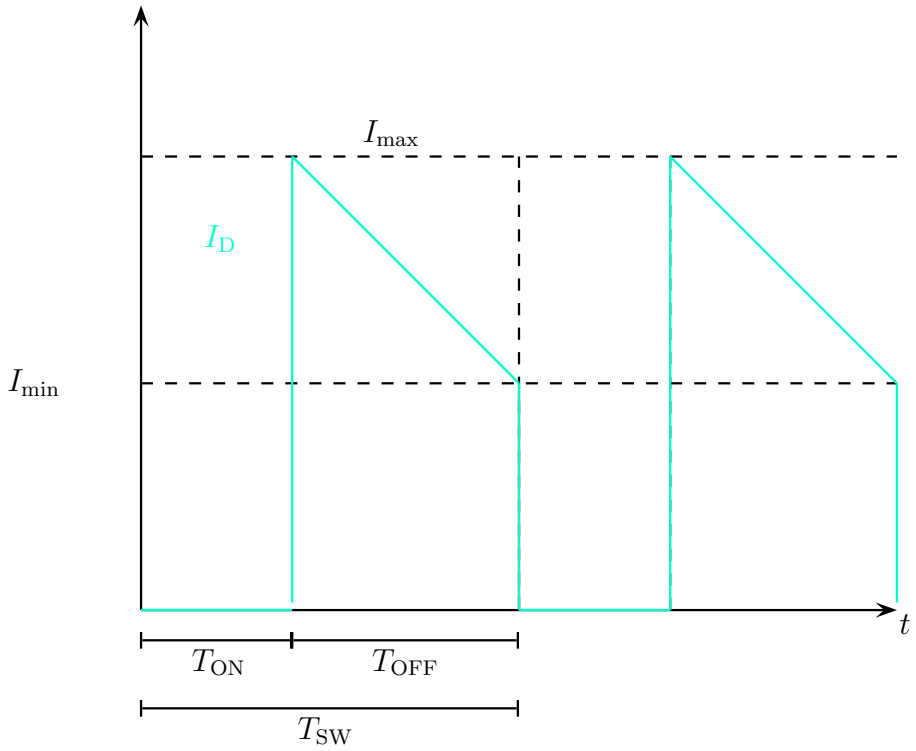
$$(1 + sC_0R_{\mathrm{S}})$$

By changing the ESR, we change the position of this zero; this zero gives us stability, because it increases the phase margin: if we change the capacitor, even the **producer**, we risk to change the ESR, making our system unstable.

All the SoB (Son of a Boost) converters have this zero at the right half-plane: these are very hard to correct, even harder than right-half-plane poles!

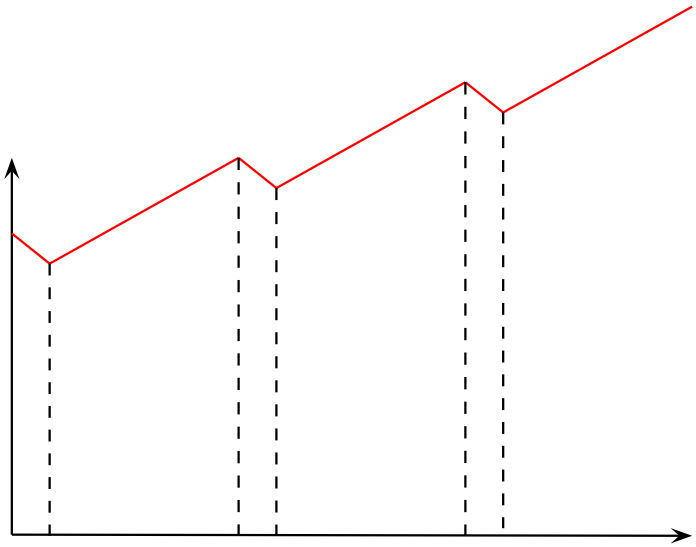
If we analyze a buck-boost converter instead of a boost converter, we have almost the same expression: maybe just different gains. Čuk converter has a more complicated transfer function, but here we can move the zero to left half-plane, changing the circuit a little bit (a sort of a snubber).

Is there some way to see a right half-plane zero? Some physical meaning? Well, let's consider a boost converter; what is I_{D}, the diode current? It is something like this:



the average of this current is just $\frac{V_0}{R}$, and it is related to the output current!

Now, let's suppose that we increase suddenly the duty cycle, in order to obtain a larger output voltage; if we do it, it happens that we increase the duty cycle, and decrease $(1 - D)$: the switch current goes up, upper respect to the previous cycle, and we obtain something like this:



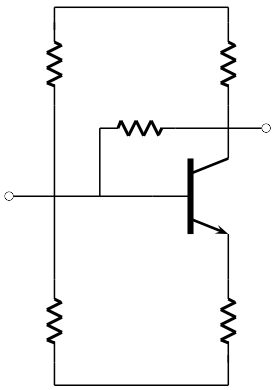
Before doing this change, the current was lower as peak, and larger. By increasing the duty cycle, what we have done is reduce $(1 - D)$, so we have less time to deliver energy to the output; eventually, these peaks will be high enough to have higher peak current, but less area: the fact that we are delivering less energy, is related to the fact that we have this right half-plane zero.

If we have an actual voltage source, things become worse: instead of two equations we have three equations, because of the added state variable.

2.2 Switch-average method

We have studied a first method to analyze a boost converter in CCM, and what we have got was the boost CCM VM (Voltage Mode), which has two moving poles (respect to d), one right half plane zero, and a left half plain zero, due to the ESR. If we repeat the same analysis for a buck-boost converter, we obtain something similar.

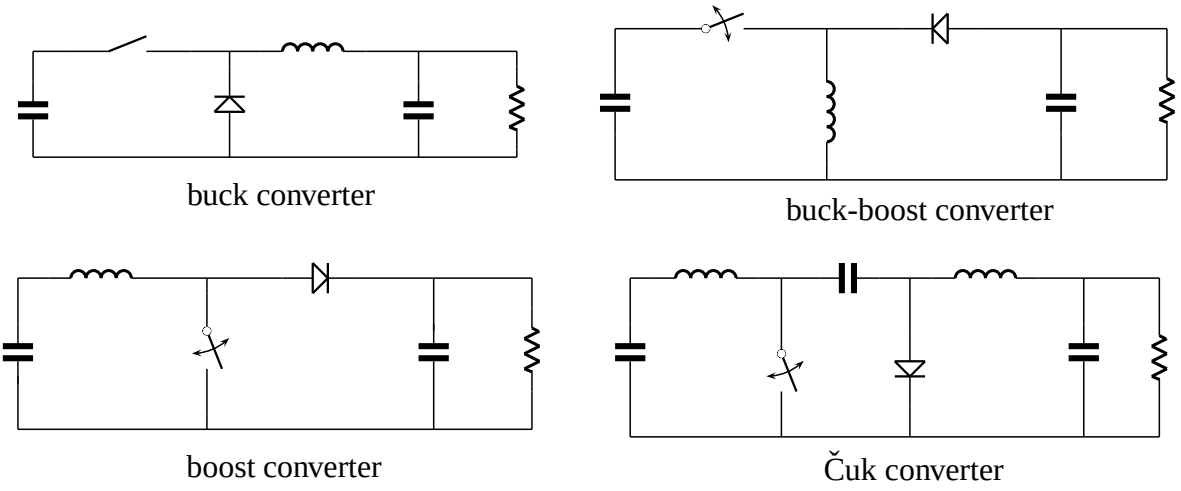
Now, we are going to introduce another method to analyze circuits: what we did last time is not the smartest way to work: we wrote down all the equations for the circuit, and did calculations; when a circuit is simple like the previous one, no problem! If we have something like this:



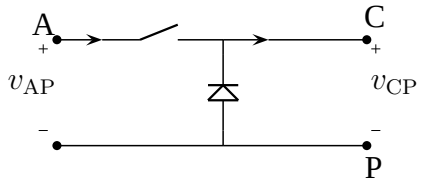
with a circuit like this we have to write down one equation for each component, and this is very boring.

When we have to study a circuit like the previous one, what we usually do? Well, we take out of the circuit the non-linear part, and substitute it with an easy model (usually, with the small-signal model, which is an LTI model); then, we can do calculations on the LTI circuit, which is more easy.

Now, we are going to introduce this method, invented by Vorperian, on a buck converter; before doing this, let's see, in the circuits we studied, which are the critical elements:



What happens in all those topologies, is that switch and diode are, in some way, connected together. So, we have to average and linearize **just the bad guys**: the switch and the diode. What to do? Well, let's start from a buck converter: we have a sub-circuit like this:



We have to average and linearize this circuit: this is the part which makes our converter time-variant (and then non-linear); as we obtain an LTI model, we can re-substitute into the former circuit, and study all the quantities we want.

In our sub-circuit we can identify three terminals: A terminal(**active** terminal, because it is the pin of the active switch); P terminal (**passive** terminal, because it is the pin connected to the diode, which is a passive switch); C terminal (**common** terminal, because it is the node between the two devices, so in common to the two devices).

A remark: generally we don't put an inductor on the node a, because if the switch opens the inductor gets mad (if we stop the current through the inductor the derivative of the current, which is proportional to the voltage across it, goes ideally to infinity); same story, if we want to put an inductor in series to the diode.

Now: considering T_{ON} (related to the duty cycle[1] d) the time when the

[1]Let's remark that we are performing a dynamic analysis, so all those quantities are variable, and we are referring to the ISO conventions

switch is closed, and so T_{OFF} the time when the switch is open (and the diode conducts), we can wrote down some equations.

- During the T_{ON} phase, so during d:

$$\begin{cases} v_{\mathrm{CP}} = v_{\mathrm{AP}} \\ i_{\mathrm{A}} = i_{\mathrm{C}} \end{cases}$$

- During the T_{OFF} phase, so during $1 - d$:

$$\begin{cases} v_{\mathrm{CP}} = 0 \\ i_{\mathrm{A}} = 0 \end{cases}$$

  in fact, during this phase, the diode is conducting, so the actual voltage equals the voltage drop on it.

Those equations are linear, time-invariant, and algebraic! Now, we don't have any differential equation, components with memory or something else.

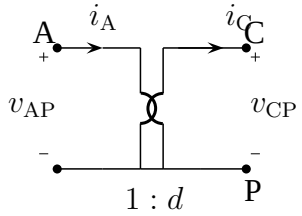
Now, we have to **average** those equations, in order to obtain just one set of equations: the weights of our equations are d and $1 - d$; so:

$$\begin{cases} v_{\mathrm{CP}} d + v_{\mathrm{CP}}(1 - d) = v_{\mathrm{AP}} d + 0 \\ i_{\mathrm{A}} d + i_{\mathrm{A}}(1 - d) = i_{\mathrm{C}} d + 0 \end{cases}$$

so, cleaning, we obtain:

$$\begin{cases} v_{\mathrm{CP}} = v_{\mathrm{AP}} d \\ i_{\mathrm{A}} = i_{\mathrm{C}} d \end{cases}$$

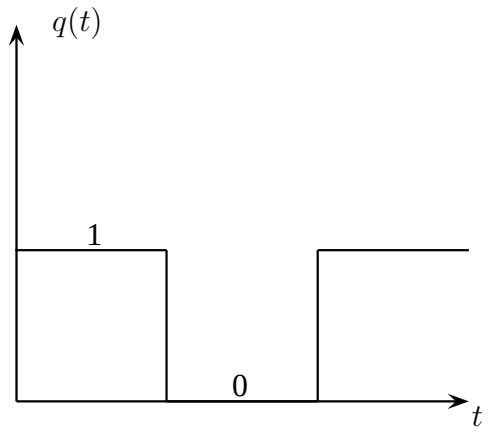
We have still two algebraic equations, but now they are non-linear: many of the terms are given by the product of two variable terms! If we re-name d to n, we obtain substantially the equations of a **transformer** (which can handle also DC values):



What do we need so? Well, we can remove our switches, and put this average model instead of our terms!

Proof of this method

We have said that all of this stuff works; we have to **prove** it! Let's consider something like this: defined a **switching function** $q(t)$ (in time domain), which describes the behaviour of the switch SW, we have something like this:



The average of this function is the duty cycle! In time domain, so without using approximations, we can write that:

$$v_{\mathrm{CP}} = q(t) v_{\mathrm{AP}}$$

and

$$i_{\mathrm{A}} = q(t) i_{\mathrm{C}}$$

let's calculate the averages of these quantities:

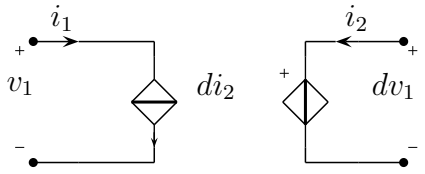
$$\begin{cases} \overline{v_{\mathrm{CP}}} = \overline{v_{\mathrm{AP}} q(t)} \\ \overline{v_{\mathrm{A}}} = \overline{i_{\mathrm{C}} q(t)} \end{cases}$$

Now, a problem: our desire is to say that the average of the product equals the product of the averages; this is not true, in general, because, in order to have this, we need **statistically independent variables**, or one constant; we actually don't have any constant value respect to another, but we have that v_{AP} and i_{C} change slowly respect to $q(t)$, due to the τ constant which is, for our hypothesis, much more larger of the switching period: we are assuming that the spectrum of the switching part and the one of the changing part are distant (this is not a great idea, but it works); so:

$$\begin{cases} \overline{v_{\mathrm{CP}}} \sim \overline{v_{\mathrm{AP}}} \overline{q(t)} \\ \overline{v_{\mathrm{A}}} \sim \overline{i_{\mathrm{C}}} \overline{q(t)} \end{cases}$$

This method is much more powerful than the state space one: we are using only simple equations, and just for the time-varying elements; the main reason is that now we are handling **circuits**, instead of a lot of equations: if we give it to a simulator like SPICE, it will calculate without problems all the quantities!

In SPICE we can introduce a model like this:



This model is non-linear, so we have to linearize it, and in order to perform this operation we can use the same trick we used before. Let's decompose all or quantities in two parts: bias point and variable part:

$$v_{\mathrm{CP}} = V_{\mathrm{CP}} + \hat{v_{\mathrm{cp}}}$$

$$v_{\mathrm{AP}} = V_{\mathrm{AP}} + \hat{v_{\mathrm{ap}}}$$

$$i_{\mathrm{A}} = I_{\mathrm{A}} + \hat{i_{\mathrm{a}}}$$

$$i_{\mathrm{C}} = I_{\mathrm{C}} + \hat{i_{\mathrm{c}}}$$

$$d = D + \hat{d}$$

If we are assuming signal condition, so if we have that:

$$V_{\mathrm{CP}} \gg \hat{v_{\mathrm{cp}}}$$

$$V_{\mathrm{AP}} \gg \hat{v_{\mathrm{ap}}}$$

$$I_{\mathrm{A}} \gg \hat{i_{\mathrm{a}}}$$

$$I_{\mathrm{C}} \gg \hat{i_{\mathrm{c}}}$$

$$D \gg \hat{d}$$

we can neglect all the second order terms, and maintain just the first order terms!

Now: let's re-write our equations with the bias + variable notation:

$$\begin{cases} V_{\mathrm{CP}} + \hat{v_{\mathrm{cp}}} = (D + \hat{d})(V_{\mathrm{AP}} + \hat{v_{\mathrm{ap}}}) \\ I_{\mathrm{A}} + \hat{i_{\mathrm{a}}} = (D + \hat{d})(I_{\mathrm{C}} + \hat{i_{\mathrm{c}}}) \end{cases}$$

so, if we expand all the terms, we obtain something like:

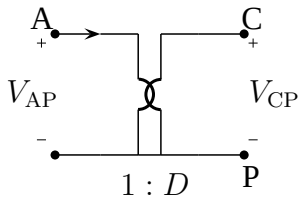
$$\begin{cases} V_{\mathrm{CP}} + \hat{v_{\mathrm{cp}}} = DV_{\mathrm{AP}} + D\hat{v_{\mathrm{ap}}} + \hat{d}V_{\mathrm{AP}} + \hat{d}\hat{v_{\mathrm{ap}}} \\ I_{\mathrm{A}} + \hat{i_{\mathrm{a}}} = DI_{\mathrm{C}} + D\hat{i_{\mathrm{c}}} + \hat{d}I_{\mathrm{C}} + \hat{d}\hat{i_{\mathrm{c}}} \end{cases}$$

Now, if we are satisfying the small-signal condition, we have just:

$$\begin{cases} V_{\mathrm{CP}} + \hat{v_{\mathrm{cp}}} = DV_{\mathrm{AP}} + D\hat{v_{\mathrm{ap}}} + \hat{d}V_{\mathrm{AP}} \\ I_{\mathrm{A}} + \hat{i_{\mathrm{a}}} = DI_{\mathrm{C}} + D\hat{i_{\mathrm{c}}} + \hat{d}I_{\mathrm{C}} \end{cases}$$

So, each equation has a DC part and two AC parts. Now, separating the two parts, we can obtain two models: the bias point model, and the small-signal model: this is like what we do studying a transistor circuit: we have a model which permits to evaluate the bias point of the circuit, and one model which can describe, starting from the bias point parameters, the behaviour of the variable part of the quantities of the circuit.

The bias point model is something like this:



where

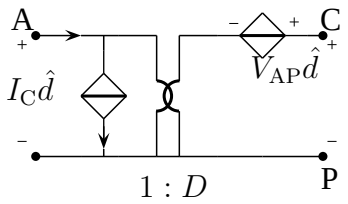
$$\begin{cases} V_{\mathrm{CP}} = DV_{\mathrm{AP}} \\ I_{\mathrm{A}} = DI_{\mathrm{C}} \end{cases}$$

What about the small signal model? Well, we have something these equations:

$$\begin{cases} \hat{v_{\mathrm{cp}}} = D\hat{v_{\mathrm{ap}}} + \hat{d}V_{\mathrm{AP}} \\ \hat{i_{\mathrm{a}}} = D\hat{i_{\mathrm{c}}} + \hat{d}I_{\mathrm{C}} \end{cases}$$

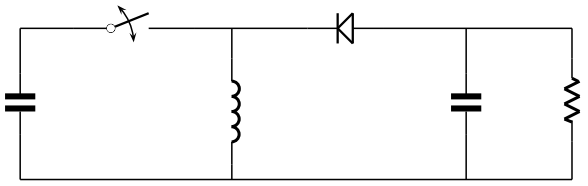
We have again a transformer, but also something else: there is at the left side another current term (which is pumping down current, because we have

that the current inside the node A is given by the sum of two contributes), and at the right side something similar, with a voltage: those effects are modelled with two controlled sources. So, this is the final small-signal model:

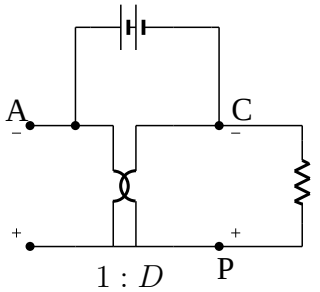


Application example: buck-boost converter

Let's try to apply this method on a converter: the buck-boost one. We have something like this:



The first step is to identify the three nodes: A, C, P; this, in order to understand how to draw the equivalent circuit. Our purpose now is just to re-draw the circuit, and obtain the bias point equivalent. We are handling DC voltages, so a capacitor is an open circuit, and an inductor is just a piece of wire; we simply have:



we can find the output voltage, using this loop: at left we have (using the transformer's equation) $\frac{V_0}{D}$, so:

$$V_{\text{in}} + \frac{V_0}{D} = V_0$$

so

$$V_0 \left(1 - \frac{1}{D}\right) = V_{\text{in}}$$

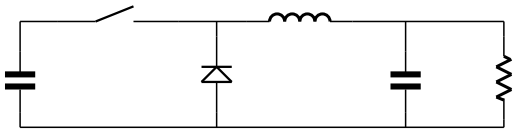
so

$$\frac{V_0}{V_{\text{in}}} = M = \frac{D}{D-1}$$

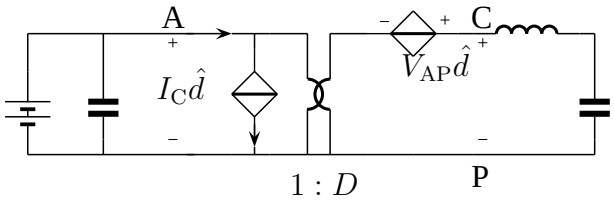
we already knew it!

2.2.1 Dynamic analysis of a buck converter

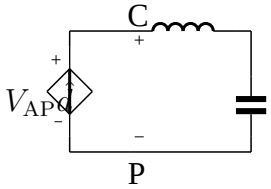
Now we are going to perform the dynamic analysis of a buck converter; the basic circuit is the following one:



We have to identify (this was already done in the last schematics) the three points A, B, C; once we have done it, we can substitute the small signal model, and obtain something like this:



In small signal model analysis, all the DC terms become null: the voltage generators (the batteries) become a short circuit. In this particular case, we have that $I_C = I_0$; the short circuit makes the current generator and the transformer be useless (it covers them), so the equivalent circuit we have to use is simply this:

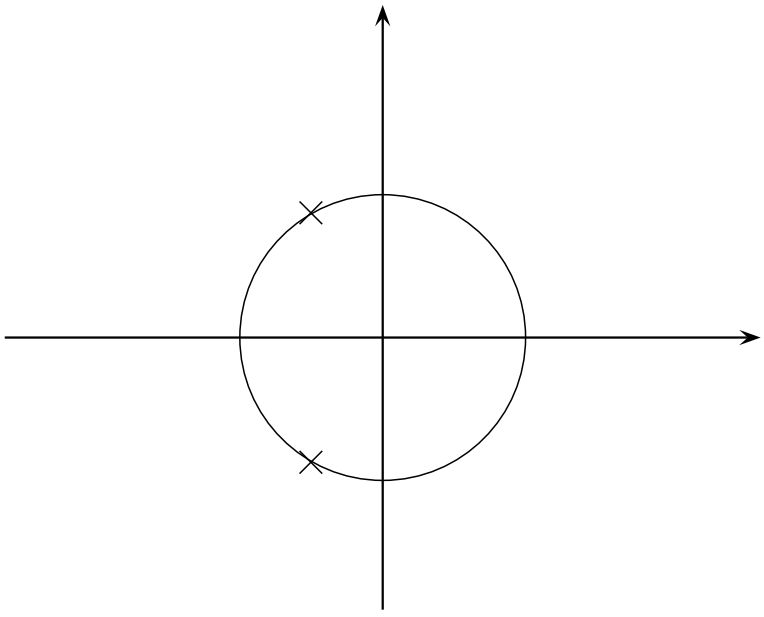


A remark: we said that, from the small-signal point of view, all the DC terms are zero; we have dependency on V_{IN}, which is zero, for the small signal, **but** V_{IN} is zero just in the circuit: it is a parameter of the bias point, and we need it in order to do the calculations! Our idea is: once we calculated the bias point parameters, we can use them in order to calculate the quantities varying around them: as we used to calculate g_{m} in a transistor circuit, now we use V_{IN} or I_{C} or other stuff to take account of the bias point, even in the small-signal model.

Now, we are looking for $\hat{v_0}$ over $\hat{d}$: this is the transfer function which uses the duty cycle as input (we are interested in it because we need this stuff to analyze the control system). We can see that this is simply a low-pass filter transfer function: by using simple circuit theory we obtain

$$\frac{\hat{v_0}}{\hat{d}} = V_{\mathrm{IN}} \frac{1}{s^2 LC + s\frac{L}{R} + 1}$$

This expression has two complex conjugate poles: those poles are moving, because R is a variable parameter (the load can change), but the frequency is just given by LC: what actually changes is just the damping, ζ!



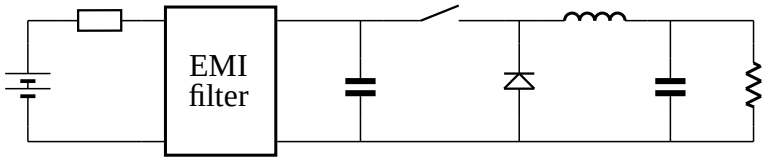
The radius of this circle is related to the ω of the poles, and their position on the circle to the ζ parameter, which changes with the load R!

Some remarks: the total gain of the circuit changes with the DC input voltage, V_{IN}; the expression calculated does not take account of the ESR R_{S}, which introduces a zero in the left half-plane of the Laplace domain:

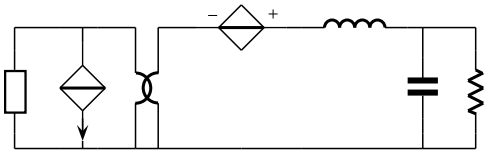
$(1 + sCR_S)$. At the denominator, we have a small change, because, instead of R, we have $R + R_S$; R_S is very lower than R, so the change is very little. The only interesting part is the zero, which depends on the parasitic ESR: it can change for many reasons: temperature, lifetime, manufacturer.

Real voltage source

What happens if our voltage source is real? Well, we have something like this:



We have an EMI filter (which can contain inductors or something else); watching back into the EMI filter, what we see is an impedance. When we introduce the model of the circuit, we have something like:



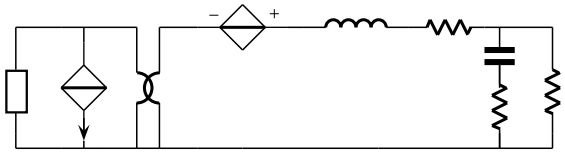
We want to remark some things: now, if we want to show $\hat{v}_0/\hat{d}$, and it will have the same denominator (unless we introduce some other extra poles with the EMI filter); at the numerator, we get something bad: when $\hat{d}$ goes up, we increase the $\hat{v}_0$ term, and ok; when we increase $\hat{d}$ what we obtain is also to increase the current through the controlled source at the left side; if we bring this current source to the right side (using the transformer's constitutive equations) we still have a generator which pulls down current, which introduces a negative contribute respect to the first one; what we expect at the denominator is that we have a positive term, and a negative term (functions of $\hat{d}$): the two terms are opposite! Another observation: Z_{in} is an impedance, a complex quantity: there will be some frequency where the negative term is the most important, another one where the positive is more important: the gain of our system will be positive in a frequency range, and negative in another frequency range! This means that feedback changes its sign with the frequency: it is the classical situation connected to a right half-plane zero!

We have to introduce an EMI filter, and it **can** introduce instability, but usually it doesn't disturb our converter; there is a paper which explains how to design the converter.

Measurements observations

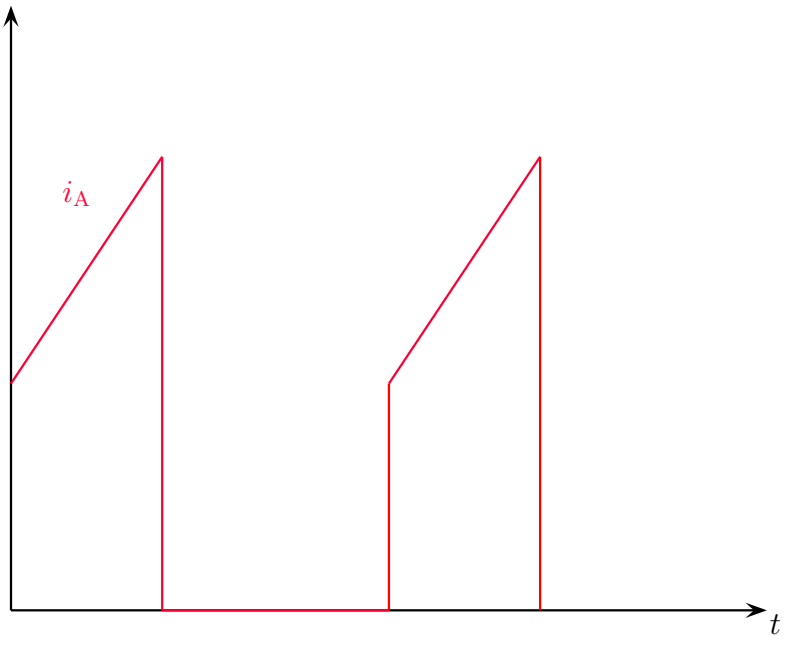
When this method was discovered, in order to verify if it works, some researchers tried to make some measurements, and discovered an interesting thing.

Let's consider this model:

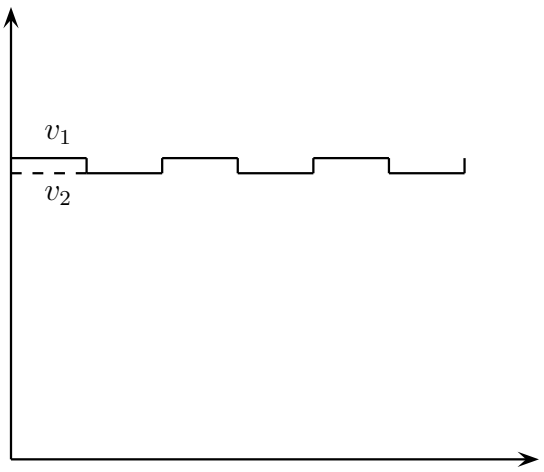


This is substantially a LC filter (with an R_L, an ESR relative to the inductor, and some ESR relative to the capacitors). The researchers discovered that the Q factor of this LC circuit in the theoretical model is higher than the actual one. Why?

Let's consider the buck converter, and the input current i_{A}, which is more of less something like this:



The average input voltage $\overline{v_{\mathrm{AP}}}$ was supposed equal to V_{IN}; actually, we have a v_{IN} which is something like this:



Why? Well, every time we close the switch, we take current from the input capacitor, which has an ESR: every time we close the switch the current produces a little voltage drop on this ESR, and we lose some input just for the reason that we are closing the switch, and performing the measurement!

When we do the average calculations, we can say that:

$$\overline{v_{\mathrm{AP}}} = V_{\mathrm{IN}}$$

this is almost true, but we have a trouble: every time we sample with our sampling system (the active switch), we reduce the level, and we sample the lower level of the voltage! It is like if we try to measure the voltage level of the distribution network with a lamp: as we turn the lamp on, the voltage decreases, because of the losses introduced by the load! Another way to understand this fact, is: we are sampling at f_{SW}, a signal which changes at f_{SW}: every time we close the switch we take the same value, because we are not satisfying Nyquist's rule.

Input voltage so behaves like a square wave, with two levels, v_1 and v_2; we already know v_1, but which is v_2 ?

Well, we have that $v_1 - v_2$ is the amplitude of the step; when we close the switch, the variation comes from the voltage drop on the ESR. We have, given the ESR R_{S}:

$$v_1 - v_2 = i_{\mathrm{C}} R_{\mathrm{S}}$$

Where R_{S} is the ESR of the **input capacitor**.

We can perform our average calculations taking account of this difference:

$$v_2 D + v_1(1-D) = \overline{v_{\mathrm{AP}}}$$

but we can substitute to v_1 what we have found:

$$\overline{v_{\mathrm{AP}}} = v_2 D + (v_2 + i_{\mathrm{C}} R_{\mathrm{S}})(1-D)$$

so, cleaning this expression:

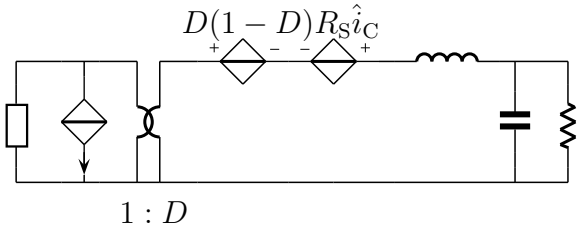
$$v_2 = \overline{v_{\mathrm{AP}}} - i_{\mathrm{C}} R_{\mathrm{S}}(1-D)$$

where $\overline{v_{\mathrm{AP}}} = v_{\mathrm{IN}}$.

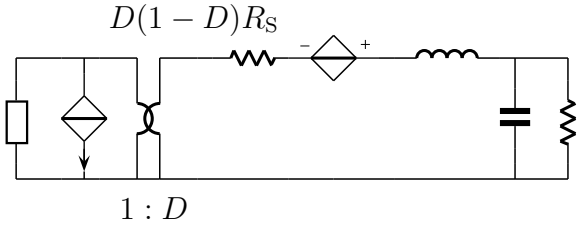
This is the actual voltage we have at the input of our converter; if we consider the small-signal approximation, we can say that:

$$\hat{v}_0 = -\hat{i}_{\mathrm{c}} R_{\mathrm{S}}(1-D)$$

This means that our signal model has one extra term; we can model it as:



We can take it at the right side of the transformer, simply by multiplying by D (the transformer ratio); the final observation is this one: we have something which has a voltage drop on it proportional to the current flowing through it: a resistance!



This is because we have the lower Q: the presence of an extra resistance in the circuit.

A remark: this a resistance which does not dissipate DC! It is just a resistance present in the small signal model! It is just an AC resistance, like the r_π for BJT or the output resistance we calculated previously, $\frac{\partial V_0}{\partial I_0}$.

Final observations

We have seen that this topology has two complex conjugate poles; what we don't emphasized is that:

$$f_{\mathrm{p}} = \frac{1}{2\pi\sqrt{LC}}$$

The capacitance value is **important**: we care about it, even if it is electrolytic: in the dynamic modelling of the circuit also μF are important!

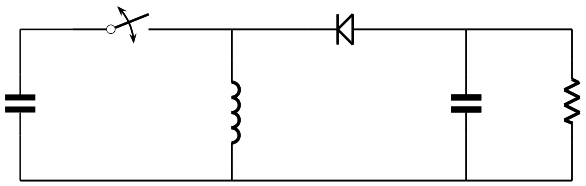
A remark: every time we have a converter with an electrolytic capacitor, so with an ESR, it introduces a zero in the left half plane of the Laplace domain.

2.3 Circuit average method - DCM analysis

We are going to analyze DCM, in a converter which is not a buck: it is stupid to use DCM in a converter which does not need it for any reason! CCM is better because it permits to reduce stresses on the components, so, if there are no control issues, why use DCM?

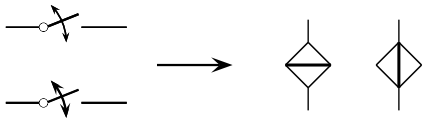
A boost converter is usually designed in DCM (unless we are designing a PFC: in this case it works with a very low frequency range, so, thanks to its short bandwidth, we can also design the boost PFC in CCM, because the right half plane zero is not important yet).

Now we are going to analyze the buck-boost converter in DCM, with a new method: the **circuit average**: this is slightly better for DCM analysis. Let's consider this schematic:



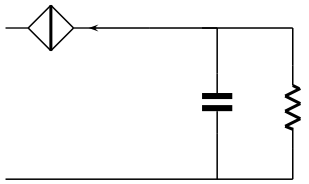
The basic idea is: we have to average it, piece by piece; a capacitor, an inductor, a resistor, are devices which realize the behaviour of a capacitance, of an inductance, of a resistance: the average value of these devices will be the values of the quantity they want to realize.

About the switch, things are different: when the switch is open, we have that the voltage across it is non-zero, and the current is zero; when it is closed, voltage across it is zero, and current different from zero (this, ideally). In order to average this bipole we need something which has on it some voltage, and some current: a controllable voltage or current source:



Voltage or current is almost the same: usually calculations can be harder or simpler with one of the two, but doesn't change so much (most of the times we will use a current source).

So: let's substitute the diode with a controlled current source:



This is the output stage of the buck-boost converter: on our sub-circuit we have a current equal to $\overline{i_{\mathrm{D}}}$. Which is the average current on the actual diode?

We know that the current on the diode has a triangular waveform; what we can do is, so, something like this:

$$\overline{i_{\mathrm{D}}} = \frac{1}{2}\frac{T_2 I_{\max}}{T_{\mathrm{SW}}}$$

Now we just have to find all the values involved in this equation. $I_{\max}$ equals:

$$I_{\max} = \frac{v_{\mathrm{IN}}}{L} T_1$$

this is known from the theory we already studied. What about T_2? Well, we can use also the other equation:

$$T_2 = \frac{I_{\max}}{-\frac{v_0}{L}}$$

but we know $I_{\max}$, from the previous equation!

$$T_2 = \frac{\frac{v_{\mathrm{IN}} T_1}{L}}{-\frac{v_0}{L}} = -\frac{v_{\mathrm{IN}}}{v_0} T_1$$

So, if we substitute in the average of the diode current, we obtain:

$$\overline{i_{\mathrm{D}}} = \frac{T_1 \frac{v_{\mathrm{IN}}}{v_0} \frac{v_{\mathrm{IN}}}{L} T_1}{2 T_{\mathrm{SW}}}$$

so, if we do some cosmetic arrangements, multiplying and dividing by T_{SW}, we easily obtain:

$$\overline{i_{\mathrm{D}}} = \frac{d^2 v_{\mathrm{IN}}^2}{2 f_{\mathrm{SW}} L v_0}$$

This is a time-invariant non-linear equation (we are performing as usual a dynamic analysis, so all our parameters have bias point and variable contributes). In order to obtain a linear model, we have to linearise this current source: one way is to use the same old way, decomposing the contributes in bias point and variable part; another way is to explicit the Taylor expansion, up to the first term, for all the variables involved in the system. We have that:

$$\overline{i_{\mathrm{D}}} = f(d, v_{\mathrm{IN}}, v_0)$$

we can expand it using Taylor:

$$\overline{i_{\mathrm{D}}} \sim \overline{i_{\mathrm{D}}}|_{\text{bias point}} + \left.\frac{\partial \overline{i_{\mathrm{D}}}}{\partial d}\right|_{\text{bias point}} (d - D) +$$

$$+ \left.\frac{\partial \overline{i_{\mathrm{D}}}}{\partial v_{\mathrm{IN}}}\right|_{\text{bias point}} (v_{\mathrm{IN}} - V_{\mathrm{IN}}) + \left.\frac{\partial \overline{i_{\mathrm{D}}}}{\partial v_0}\right|_{\text{bias point}} (v_0 - V_0) =$$

$$= \overline{i_{\mathrm{D}}}|_{\text{bias point}} + \left.\frac{\partial \overline{i_{\mathrm{D}}}}{\partial d}\right|_{\text{bias point}} \hat{d} + \left.\frac{\partial \overline{i_{\mathrm{D}}}}{\partial v_{\mathrm{IN}}}\right|_{\text{bias point}} \hat{v_{\mathrm{in}}} + \left.\frac{\partial \overline{i_{\mathrm{D}}}}{\partial v_0}\right|_{\text{bias point}} \hat{v_0}$$

These three derivatives are **numbers**, because they are evaluated in a specific case: around the bias point! Let's define three parameters:

$$A \triangleq \left.\frac{\partial \overline{i_{\mathrm{D}}}}{\partial d}\right|_{\text{bias point}} = \frac{2 D V_{\mathrm{IN}}^2}{2 L f_{\mathrm{SW}} V_0} = \frac{D V_{\mathrm{IN}}^2}{L f_{\mathrm{SW}} V_0}$$

$$B \triangleq \left.\frac{\partial \overline{i_{\mathrm{D}}}}{\partial v_{\mathrm{IN}}}\right|_{\text{bias point}} = \frac{2 D^2 V_{\mathrm{IN}}}{2 L f_{\mathrm{SW}}} = \frac{D^2 V_{\mathrm{IN}}}{L f_{\mathrm{SW}}}$$

$$C \triangleq \left.\frac{\partial \overline{i_{\mathrm{D}}}}{\partial v_0}\right|_{\text{bias point}} = -\frac{D^2 V_{\mathrm{IN}}^2}{V_0^2 2 L f_{\mathrm{SW}}}$$

Let's write down this last coefficient in a different way; if we remember that, for the cyclostationary condition, we had that

$$\frac{V_0}{V_{\mathrm{IN}}} = D \sqrt{\frac{R}{2 L f_{\mathrm{SW}}}}$$

we have that:

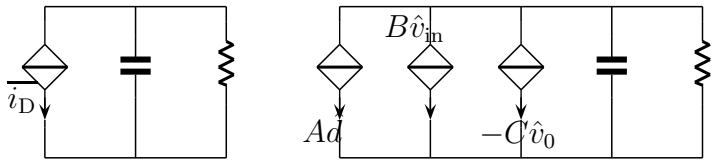
$$\left(\frac{V_0}{V_{\text{IN}}}\right)^{-2} = \frac{2Lf_{\text{SW}}}{D^2R}$$

substituting into C, we obtain:

$$C = -\frac{D^2}{2Lf_{\text{SW}}}\frac{2Lf_{\text{SW}}}{D^2R} = -\frac{1}{R}$$

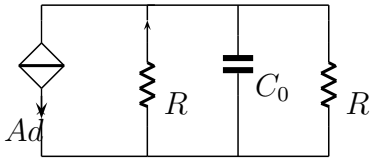
this coefficient is just a conductance, the reciprocal of a resistance! We already found this result, when we analyzed the output resistance!

After the linearisation process, we have this equivalent circuit:



Now we have a linear circuit: this means that we can use the superposition principle!

We have two input variables: $\hat{d}$ and $\hat{v}_{\text{in}}$; what we can do is to **set** to zero the input voltage $\hat{v}_{\text{in}}$, because it is useless for our purpose (obtain the transfer function to control):



We have that V_0 is negative to positive; using this convention, the coefficient $C = -R^{-1}$ becomes positive: it was negative just because we didn't consider the negative sign of v_0: if we consider this, now current on C goes **up**, respects the convention, and we can remove the sign. By simple algebra, we have to calculate $\hat{v}_0$, as:

$$\hat{v}_0 = -A\hat{d}\frac{R}{2}\frac{1}{1+sC\frac{R}{2}}$$

this, because we have two R resistances in parallel. If we substitute the value of A and divide by the variable duty cycle both the members, we obtain:

$$\frac{\hat{v}_0}{\hat{d}} = -\frac{R}{2}\frac{DV_{\text{IN}}^2}{Lf_{\text{SW}}V_0}\frac{1}{1+sC\frac{R}{2}}$$

An idea: by some algebraic manipulations, we can compact this coefficient, remembering the relation:

$$V_0 = V_{\text{IN}} D \sqrt{\frac{R}{2 f_{\text{SW}} L}}$$

Is it true? Am I allowed to use this expression into the dynamic behaviour? Well, we can do an *a posteriori* proof, considering $s \to 0$ (using so the final value theorem, relative to the Laplace transform operator); what we can do is observe that this is the A coefficient, so a coefficient relative to the **bias point** of the circuit, evaluated in the bias point, so it is related to the parameters we want to substitute.

Now, let's obtain a different expression; for $s \to 0$:

$$\frac{\hat{v}_0}{\hat{d}} = -\frac{R}{2} \frac{D V_{\text{IN}}^2}{L f_{\text{SW}} V_0} = -\frac{D V_{\text{IN}}^2}{L f_{\text{SW}}} \frac{R}{2} \frac{1}{D V_{\text{IN}}} \sqrt{\frac{2 L f_{\text{SW}}}{R}} = -V_{\text{IN}} \sqrt{\frac{R}{2 L f_{\text{SW}}}}$$

So, we have:

$$\frac{\hat{v}_0}{\hat{d}} = -V_{\text{IN}} \sqrt{\frac{R}{2 L f_{\text{SW}}}} \frac{1}{1 + sC\frac{R}{2}}$$

What we have forgot? Well, the ESR! If we want to take account of it, we have:

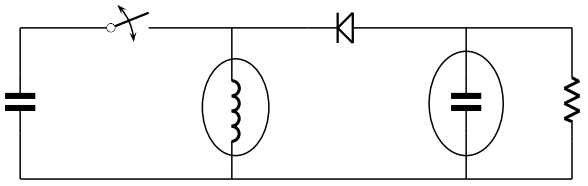
$$\frac{\hat{v}_0}{\hat{d}} = -V_{\text{IN}} \sqrt{\frac{R}{2 L f_{\text{SW}}}} \frac{1 + sCR_{\text{S}}}{1 + sC\left(\frac{R}{2} + R_{\text{S}}\right)}$$

So, for the buck-boost converter in DCM, we have a pole and a zero:

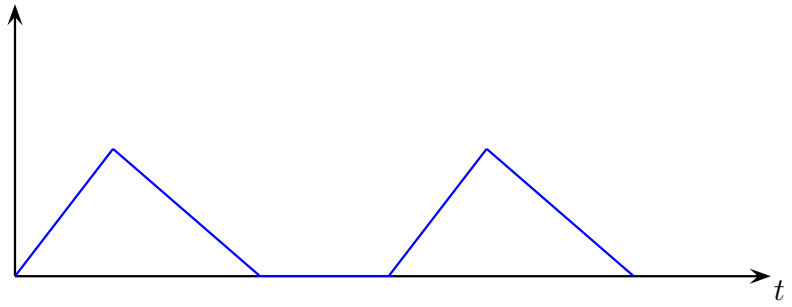
$$f_{\text{p}} = -\frac{1}{\pi R C}$$

$$f_{\text{z}} = -\frac{1}{2\pi C R_{\text{S}}}$$

Let's watch our circuit:



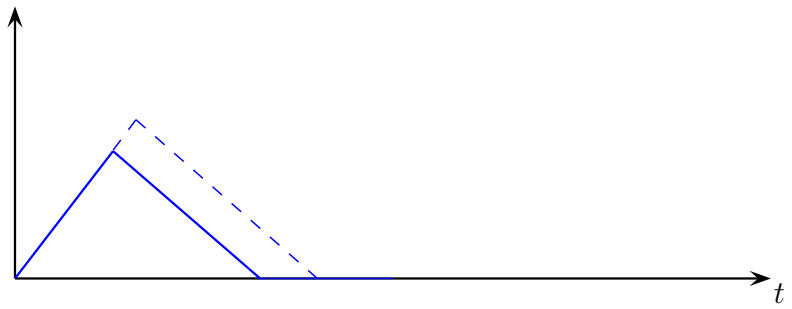
we have two dynamic elements, and just one pole and one zero! Where is the second pole? Well, we said that having a pole corresponds to have memory, store energy, and something else: what we can say is that our inductance has a current which starts from zero, increases, and then comes back to zero, before the end of the cycle: at each cycle the memory is erased, the energy is released. Saying that the circuit has short memory, means that it has a short time constant, so that it is at a very high frequency: this is a fast decaying pole, an exponential with a short time constant, so this is above $\frac{f_{SW}}{2}$, so over what our model can handle: our model can handle just up to half of the switching frequency!



So: for boost converter we have one moving pole, and one ESR zero: the L pole is at high frequencies, so our model doesn't work.

What about this result? We don't have the right half plane zero, and this is amazing! We don't have particular issues to control this circuit!

Is the right half plane pole actually disappeared? Well, in DCM it happens that, if we analyze i_L, there is something like this:



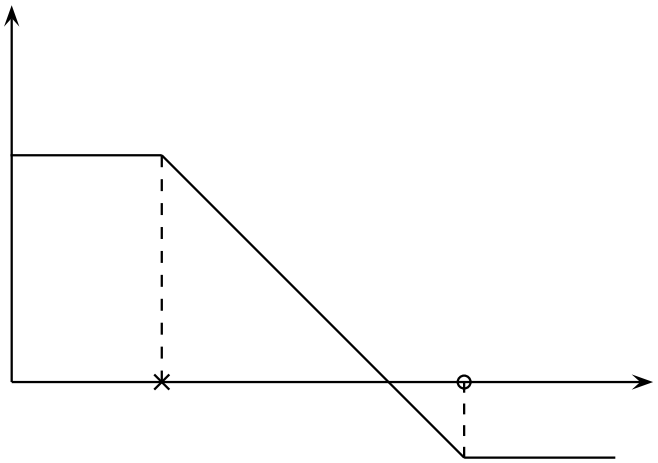
If we suddenly increase the duty cycle, it happens that the current increases, and then decreases with the **same decreasing slope** it would have: our output will get more energy! We get more energy, with an increasing duty cycle, so we don't have the effect of the right half plane zero! Actually we have it, but it doesn't influence in any way our system! We have more

time to charge the system, but also more energy, and this does not happen in a system with a right half pole zero!

During T_{ON}, the load is supplied by the right capacitor, which is designed to maintain the output voltage to a certain level. If we have an extra delay, due to the increase of the duty cycle, the capacitor loses too much charge, and we have a little output voltage decrease, due to the right half pole zero: does it matter? No! It is at a very high frequency, so it doesn't matter! This because this lasts for a very short fraction of cycle: after this fraction we have the ordinary voltage!

2.3.1 Final observations

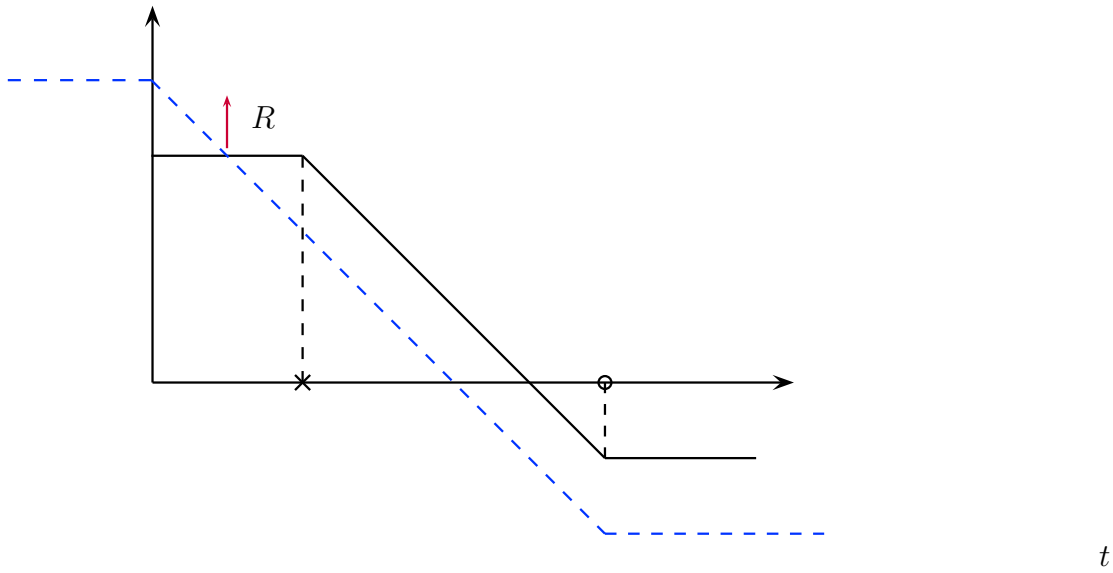
Our transfer function has one pole and one zero:



$$\frac{\hat{v}_0}{\hat{d}} = -V_{\mathrm{IN}} \sqrt{\frac{R}{2Lf_{\mathrm{SW}}}} \frac{1 + sCR_{\mathrm{S}}}{1 + sC\left(\frac{R}{2} + R_{\mathrm{S}}\right)}$$

Which conditions on my variables give us the maximum DC gain? Maximum R, maximum V_{IN}. What happens if R goes up? Well, we have that the DC gain increases, but at the same time the position of the pole decreases of a factor equal to the square of the increase of the DC gain (one depends on the square root of R, the other on R).

What does it happen? Well, the zero position is always the same: it depends on R_{S}: as we increase (in logarithmic units) with R, the frequency of the poles goes left of the double of what we gained; what happens is something like this:

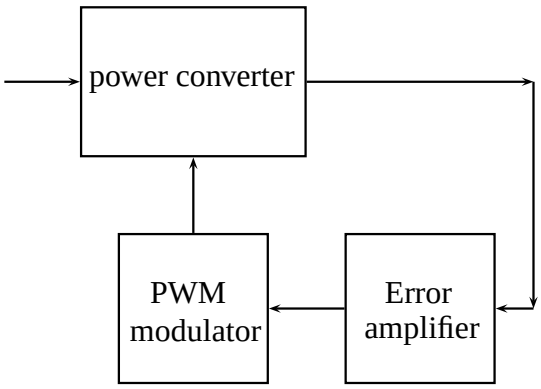


2.4 Design of the controller

The basic topologies on which we are interested to design a controller, are: buck converter in CCM, boost converter in CCM (only for PFC case), sometimes boost converter in DCM (actually, few times) and buck-boost converter in DCM. This last one is one of the most used converters, especially in its isolated version (the flyback converter): it is very cheap, even if it is a low-power converter.

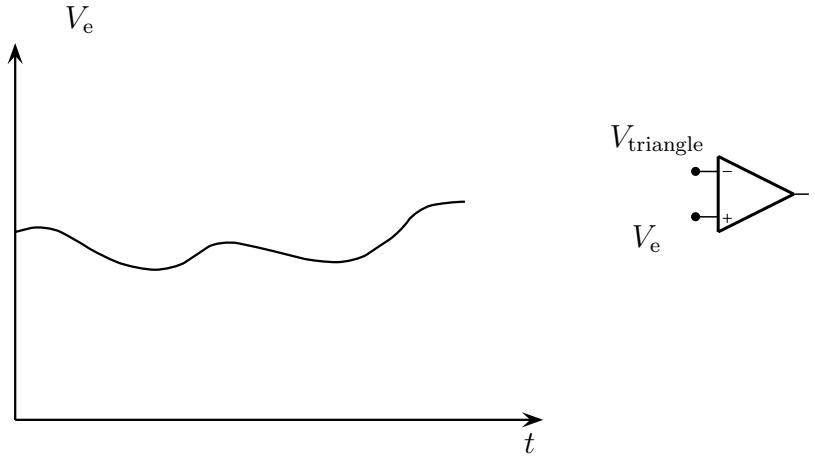
2.4.1 Some preliminary aspects

Our control part needs at least two blocks: given our power converter, we need an error amplifier, which samples the output voltage, compares it to a reference voltage, and so changes the duty cycle which drives the MOS switch.

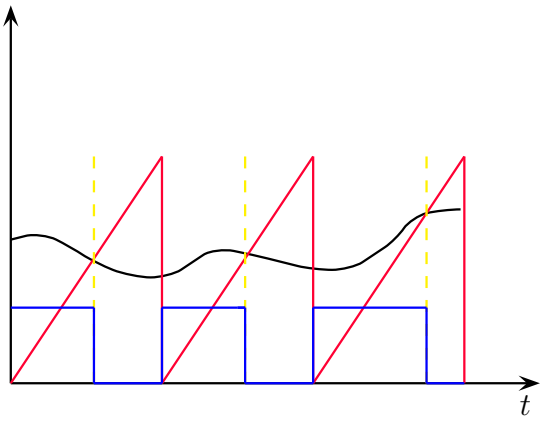


The error amplifier gives an error signal, and, in order to translate it into a digital signal, we need a PWM (Pulse Width Modulation) modulator: this is substantially a circuit which generates a duty cycle starting from an analog signal. At the input of the PWM modulator we have a voltage, and out of it a duty cycle: dimensionally, this is the reciprocal of a voltage, so its unit is V^{-1}. If the system has a gain in volts, and we are multiplying it for the reciprocal of volts, what we obtain as loop gain is dimensionless!

How can we realize this block? Well, we need something like this:

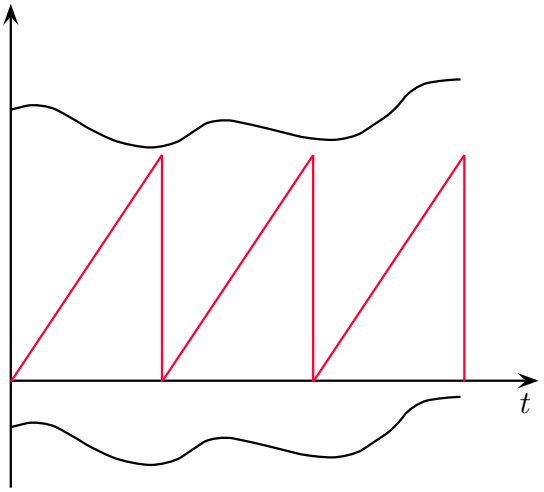


in the non-inverting input we introduce the signal from the error amplifier (which will be designed later); in the inverting input we introduce a sawtooth waveform. How does it work? Well, we have something like this:

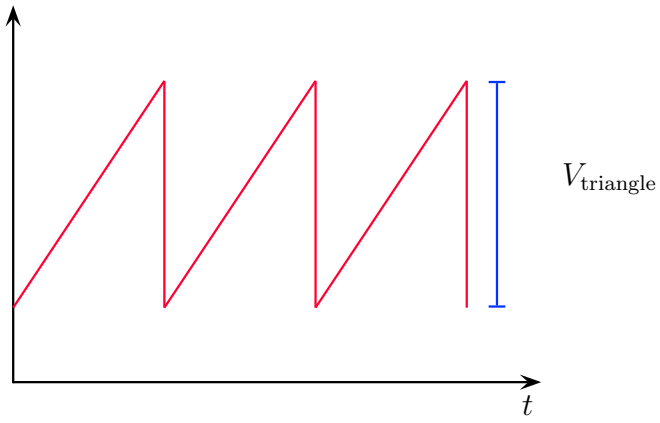


What we get in the output is a signal which is higher or lower respect to the input, so the duty cycle increases or decreases, because pulses have different width! This is called **natural PWM modulator**.

A remark: if the signal is too high respect to the maximum value of the sawtooth, the duty cycle is all the times equal to 100% ; dually, if it is all the times under the minimum value of the sawtooth, it is about 0%.



In general we have a waveform like this one



where input voltage can span through this range, and change the duty cycle.

Which is the gain for this natural modulator? Well, gain G_{PWM} can be defined as the derivative of the output quantity respect to the input quantity; the input quantity is the signal V_{e}; the output quantity, which is the duty cycle, changes linearly, because the width of the output signal depends linearly on the amplitude of the input signal. We can say that:

$$G_{\text{PWM}} = \frac{1}{V_{\text{triangle}}}$$

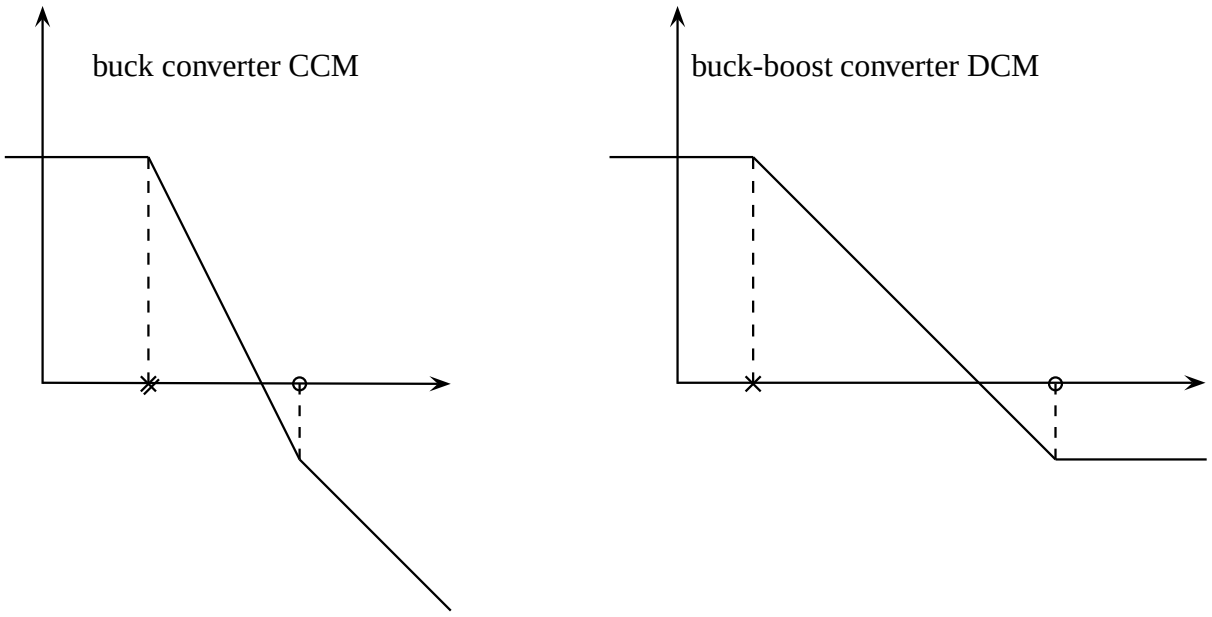
this can be explained: if we have a triangular waveform with amplitude equal to 1 V, we need a change of input voltage of 1 V in order to go from the 0 % to the 100 % of duty cycle; offset is not important.

Standard controls have a voltage almost equal to 3 V (of amplitude of the triangular waveform); for modern controllers it is smaller, due to the voltage decrease in the new processes: we can reach also 1 V.

Some remarks: if we use this PWM modulator, we have no phase delays, no poles, no zeroes; there are other kinds of PWM modulators, which have these issues. In switch mode power supplies the PWM modulator uses a sawtooth wave; in power inverters (where as inverter here we are meaning the DC to AC converters, used for driving motors) PWM has usually a symmetrical triangular waveform.

2.4.2 A theoretical introduction to our controls

Let's put together power converter and PWM modulator, in order to realize our controls. Basically, we have to handle two families of transfer function to control:



For buck CCM, the gain at low frequency is:

$$M_{\text{buck,CCM}} = \frac{v_{\text{IN}}}{V_{\text{triangle}}}$$

and for buck-boost DCM, we have:

$$M_{\text{buck-boost,DCM}} = \frac{v_{\text{IN}}}{V_{\text{triangle}}}\sqrt{\frac{R}{2Lf_{\text{SW}}}}$$

So, we want to design, starting from these equations, a closed loop system; we want to design a reasonable loop gain T, in order to have the performances we want. The basic idea we will use, is to have as loop gain T an **integrator**; this choice has some notes, we have to remember (advantages, disadvantages and some remarks):

- an integrator has high low-frequency gain: this, because the higher is the crossover frequency (the frequency at which T equals 0 dB), higher is the gain at low frequency; this, basically because the loop gain has one pole in the origin (it is a **type 1 system**); an advantage of this point is that having a type 1 system means having **no DC error**: gain is so high that we don't have to worry about DC errors.

- phase margin is about 90°, and this also at the cross-over frequency: in order to get instability, we have to delay of others 90°; this points needs

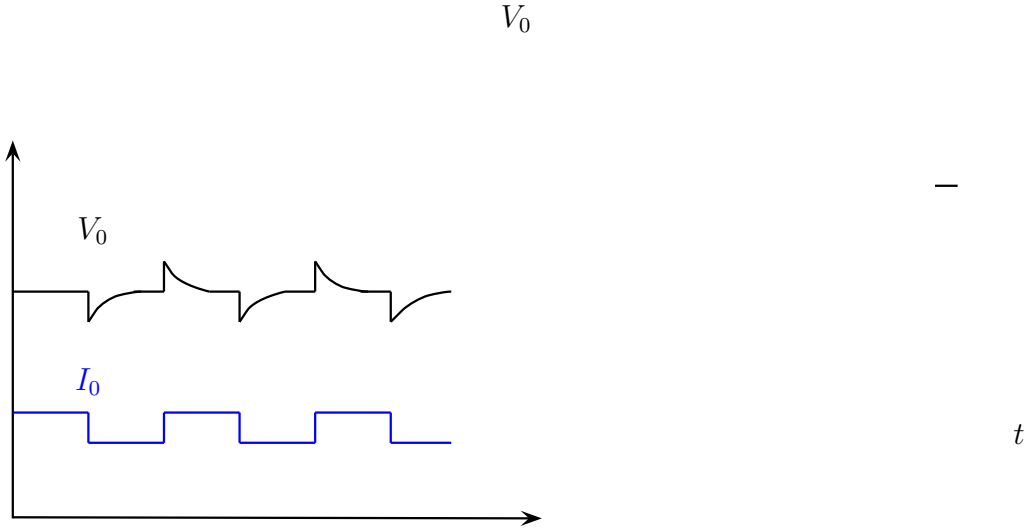
some more explanations: 90° is not a good margin, because this means that our dynamic response is quite slow; actually, if we try to design a controller with this margin, we have something like 50° (or similar) of phase margin, which is a good margin: this is not a conservative choice as it seems;

- the crossover frequency, f_c, must be **at least** one half of the switching frequency (in order to have valid models: after half of the switching frequency, we are unsatisfying the Nyquist's rule, so our model does not work); actually, we choose a crossover frequency like:

$$f_c \in \frac{f_{SW}}{6 \div 10}$$

this, because we don't want to inject noise into our system: we are doing some kind of voltage comparison, and if we have noise at this time, we have feedback problems.

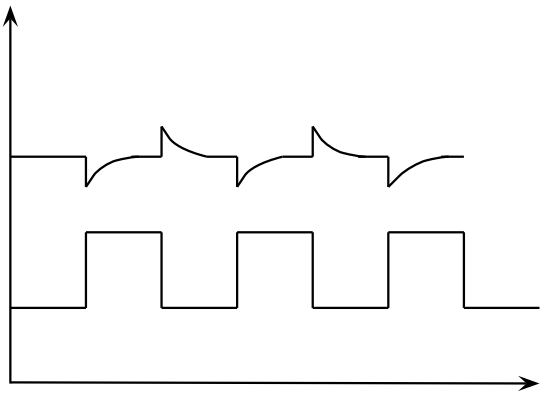
Let's discuss this last point: if we increase f_c our system will be faster to recover from bad states, like load changes, but it will be more susceptible to noise. Our I_0 behaves like this:



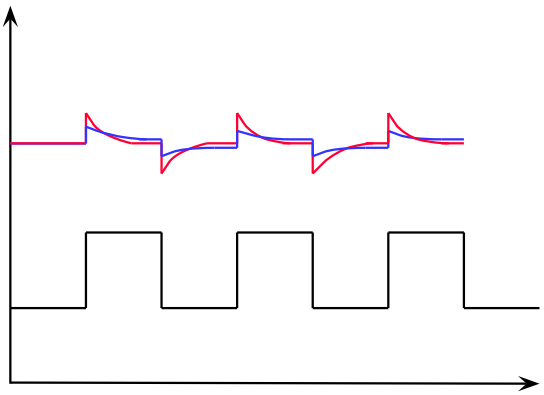
if load increases, I_0 goes up, so V_0 goes down, and the control tries to increase the duty cycle; what we obtain is the previous time response. How much is the exponential duration? Well, we can evaluate it by evaluating τ, which is:

$$\tau = \frac{1}{2\pi f_c}$$

again f_c: higher is the crossover frequency, lower is τ. The actual time behaviour of the waveform can be different: maybe we have other poles, so we can have something like



if our margin is less than 90°, it means that we have more than one pole in our system, and the behaviour **may** be this. High f_c means lower τ, unless one case: if we have two switch mode power supplies, we can have a behaviour like this:



one waveform has DC errors, because it has low gain, and the other one has more peaks; which is better? Well, it **depends**:

- if we emphasize the fact that our system must have a little integral error, so it means that we have to compare the area up and down to the average of the value:

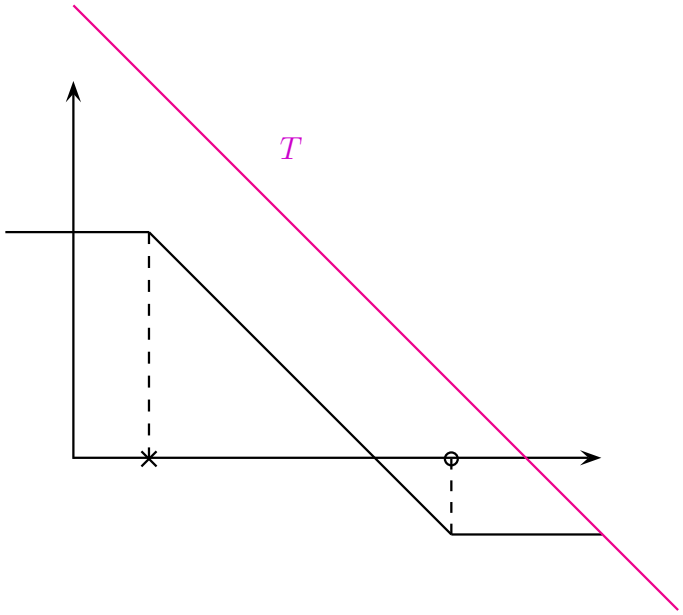
$$\int |V_{\text{actual}} - V_{\text{nominal}}|$$

in the waveform without DC errors, we have less problems, because those peaks are here for a very short time, so don't change too much the integral error;

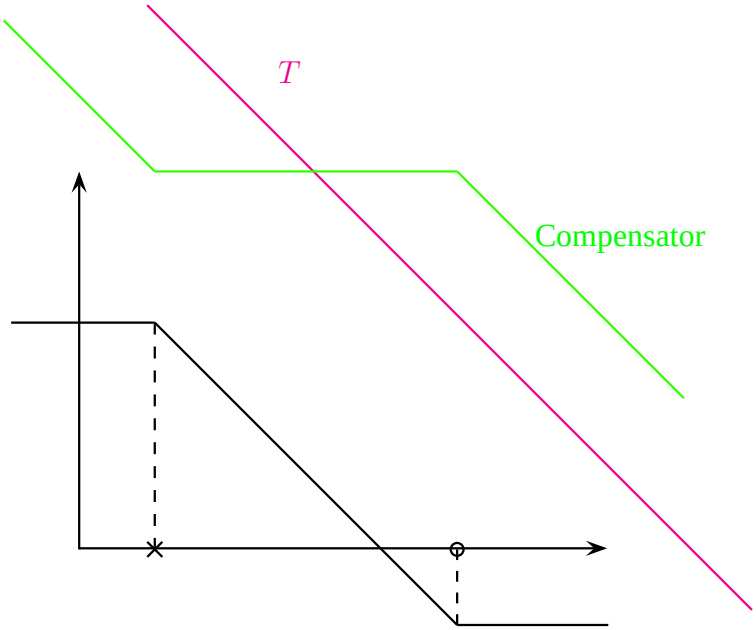
- the other waveform has an advantage: its peaks are lower, so if we have to drive something with a voltage which must not be very precise, but stay absolutely in a certain range, it is the best choice: doesn't matter how long are those peaks, because if we are driving for example a microprocessor, working at high frequency, it surely will sense the peaks, and may be damaged.

Buck-boost converter DCM case

Now, how can we design this error amplifier? Well, let's study all this stuff with a theoretical point of view: we know the behaviour of the transfer function of a converter (here we are considering a buck-boost converter); we have something like this:



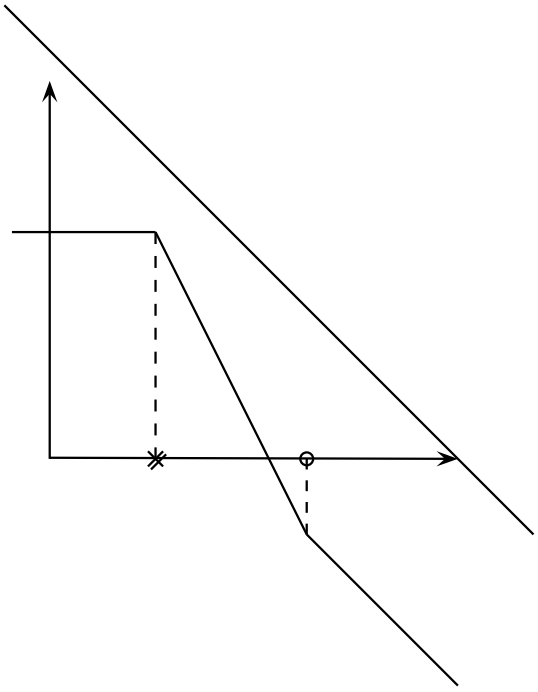
we know which is our desired final loop gain T, and the transfer function. How can we design this controller? Well, easy: simply, we can see what we have in the actual transfer function, and add some gain, some poles and some zeroes, in order to obtain that the product (which is the sum in the Bode plot) of the transfer function and of the control function equals the desired loop gain (ideally). What is missing from one curve to the other? Well, something like this:



we first introduce a pole in the origin, in order to go down with 20 dB/dec, until the transfer function reaches its pole; at this point we add a zero to the control transfer function, because we have to go down with the slope which we already have with the basic transfer function; then, again, another pole, when we reach the zero of the transfer function of the controller.

Buck converter CCM case

What about buck converter? Well, we have something slightly difficult:

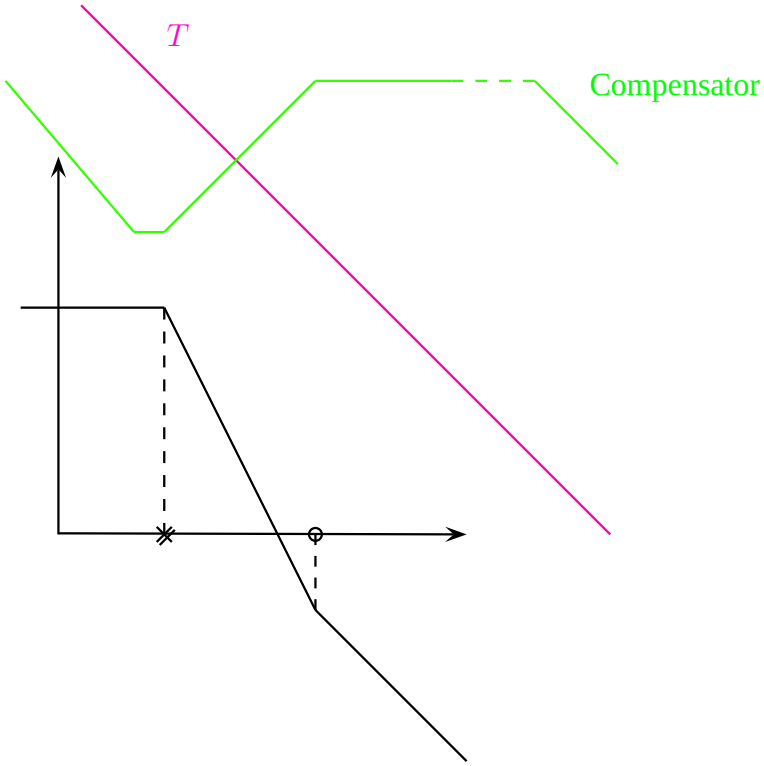


What should our compensator provide? Well, it must start with the usual pole in the origin, so introduce two zeroes, and a pole when the slope of the transfer function of the buck controller becomes equal to - 20 dB/dec.

How can we introduce those zeroes? Well, we can basically follow two ideas: two complex zeroes, or something different. If we try with two complex zeroes, and consider a system like this one: at the crossover frequency, we have 90° of phase margin: this is a very stable system. Someone can think that, when loop gain is larger than 1, phase margin is negative! This system is **stable**: phase margin is right, gain margin is a liar! Gain margin is not saying the truth: this system is stable!

There is a problem: this can be the transfer function of a buck power supply, and we know that the gain of its transfer function depends on v_{IN}: if it decreases too much, and we have that the interception with the 0 dB axis is before the poles, this system becomes **unstable**: systems like these are called **marginally stable**, because a simple change of the gain can bring this system to instability. There are cases when voltage goes low: the start-up of the converter! When we have the starting transient, the voltages of the system don't step-up, they ramp up, so we can stay locked into the unstable situation, and we don't have to risk something like this!

The solution to this fact is to use two real zeroes instead of a single zero, and to put them by this way: one, before the two poles, and one in proximity to the poles.



Why all this problems? Well, we have to check the phase: the phase of a zero is $+90°$, and it increases in two decades (from one decade before the pole to one decade after the pole); what about the phase of two conjugate poles? Well, it decreases of $180°$, but we don't know how! It depends on the damping factor of the poles! If the Q of these poles is very high, phase goes down steeply, quickly! This means that we have to avoid to have too much phase shift from the poles, and one method is to put our zero in a position which can compensate most of the phase before it shifts! The second pole will help the first one, but it will have *less work* (and avoid a marginal stability situation).

Just one more fact: our compensator, from f_c, has constant gain; this is not good, because this means that it injects noise into our loop. What we have to do is to put a pole around $\frac{f_{SW}}{2}$, in order to decrease noise. This pole **is not aimed** to control the system, but **just to decrease its bandwidth**: this pole is called **closure pole**.

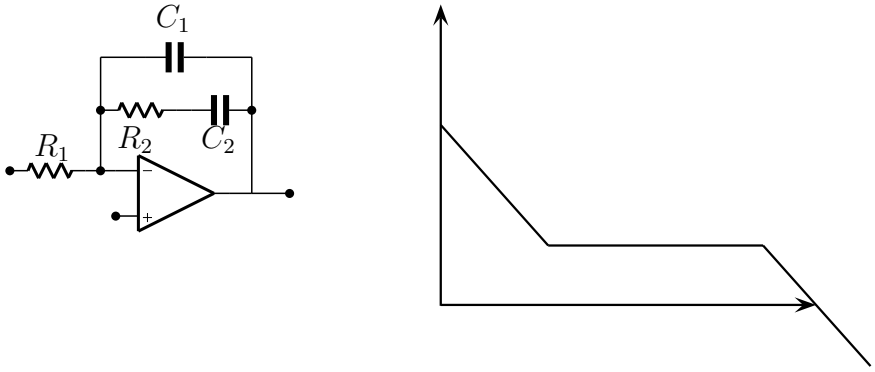
A remark: the standard name convention for power electronics community is: call each compensator with a name depending on the number of poles it has. The previous (relative to buck-boost DCM) compensator is called **type 2 compensator**, because it introduces just two poles; this one is called **type 3 compensator**, because it has three poles. Control guys

call the first controller **PI controller**, because it has an integrative part, and a proportional part (before the last pole); this second compensator is called (from control guys) PIP compensator (Proportional Integrative Proportional). Usually we want to design type 2 converters: type 3 converters are used just for buck converter in CCM: almost everything else can be controlled by a type 2 compensator.

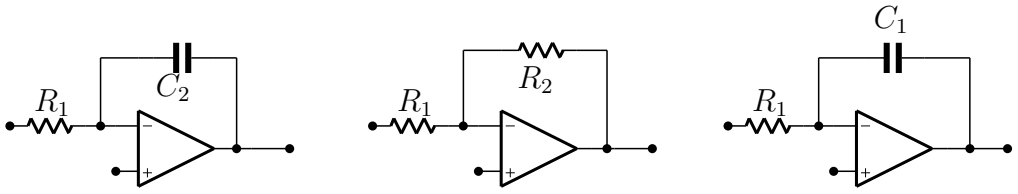
2.4.3 Practical control: compensators

Type 2 compensator

How to design in practice those compensators? Well, let's start from the simplest case: the type 2 compensator. The solution we will use is this one:



it has this behaviour, which can be represented in three phases: in the phase 1 we have that C_2 has an impedance very larger respect to R_2, so we have substantially an integrator; C_1 is much more higher than C_2 as equivalent impedance (so as values $C_1 < C_2$), and we have that it is almost open. In the second phase the impedance of C_2 becomes smaller respect to the R_2 one, so our circuit behaves like an amplifier (this is the **proportional** phase); in phase three, again, we have an integrator, with C_1 as integrating capacitance.



This is a simplified (actually, not so simple) analysis: if we calculate the transfer function of the former circuit we can obtain similar (but less approximated) results. Approximating, we can see that:

$$A = -\frac{R_2}{R_1}$$

The frequency of the zero is that frequency for whom (between phase 1 and phase 2) the impedance of the R_2 resistance equals the impedance of the C_2 capacitance:

$$R_2 + \frac{1}{sC_2} = 0$$

this, because output voltage depends basically on the voltage across this impedance; if this voltage is zero, we have a transmission zero; this occurs for:

$$f_z = -\frac{1}{2\pi R_2 C_2}$$

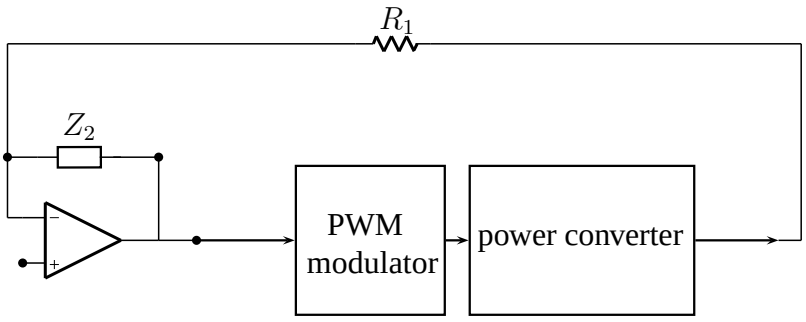
about the last pole, we have:

$$f_p = \frac{1}{2\pi R_2 C_1}$$

We have three specifications, and four components, so we need one more condition: the common sense! What we can do is to take one value for one component and design all the other starting from the specifications. A good suggestion is: start choosing the C_1 value! If values are too high, the op-amp is not able to drive it; if it is too low, parasite components become higher than the good ones. So:

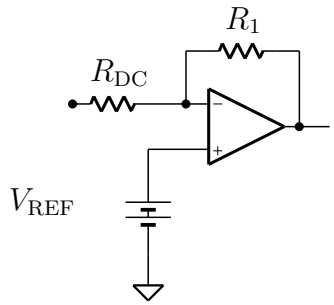
$$C_1 \sim 68\text{pF} \div 330\text{pF}$$

One more thing: let's consider this schematic (equivalent to the one previously shown):



We forgot to ask for a constant output voltage: until now, we just worried about the loop gain. All our compensator and power stage can be thought as some kind of power operational amplifier: the Z_2 impedance is some kind of *internal compensation*.

How can we control the DC output voltage, with this system? Well, let's take account of this last idea:



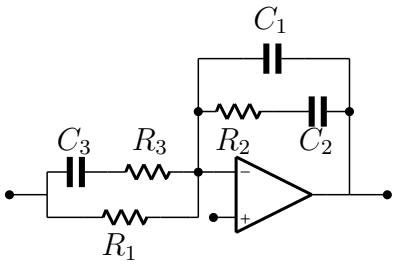
we know that:

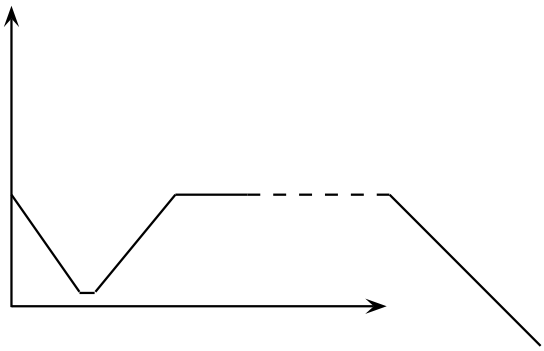
$$V_0 = V_{\mathrm{REF}} \left(1 + \frac{R_1}{R_{\mathrm{DC}}}\right)$$

this R_{DC} is a resistance which is **out of the feedback loop**: it does not change in any way the behaviour of the converter, but it fixes the output voltage at a desired value. It must be not approximated, because on it depends the output voltage: it must be chosen with a very precise value.

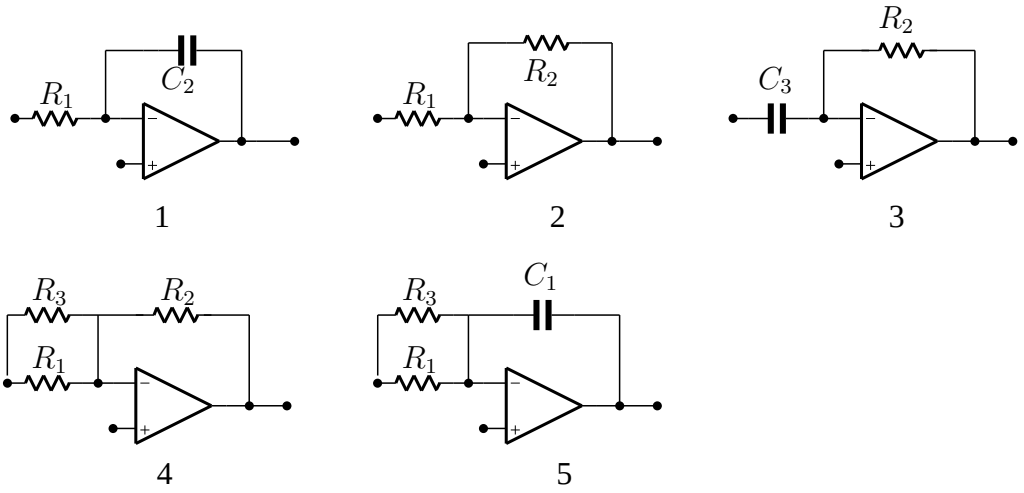
Type 3 compensator

Now, let's see how to realize in practice the type 3 compensator. We have a circuit like this:





Now we have six elements to find, and five specification (the gain A_2 depend on A_1 and on the various frequencies). Considering an idea like the previous one, we can see that there are five phases: the first two phases are equal to the first two of the previous converter; the third phase is a **derivative** phase: we have that the impedance of C_3 is higher than the impedances of R_3 and R_1; then, C_3 in phase 4 *closes* itself, and we have another gain phase (proportional phase); then, in phase 5, we have the last integrative phase.



By approximating and by using the same ideas, we have:

$$f_{\mathrm{p3}} = \frac{1}{2\pi C_1 R_2}$$

$$f_{\mathrm{p2}} = \frac{1}{2\pi C_3 R_3}$$

$$f_{\mathrm{z2}} = \frac{1}{2\pi R_1 C_3}$$

$$f_{\mathrm{z1}} = \frac{1}{2\pi C_2 R_2}$$

$$A_1 = -\frac{R_2}{R_1}$$

$$A_2 = -\frac{R_2}{R_1 \oplus R_3}$$

Some notes about compensator design

Let's start with an observation: the buck transfer function changes with the input voltage, and with the load! This means that it could be difficult to find conditions to design our converter! Without DSP or something similar, we can not realize an adaptive design (unless some particular cases). When transfer function changes, f_c changes, so we have to check that it stays into a well defined limit. Actually, it have to stay **below** a certain limit. Let's consider an example: if a buck converter works for example at 200 kHz, we have that $f_{SW} = 200$ kHz; this means that, if we divide by 6 (already explained why):

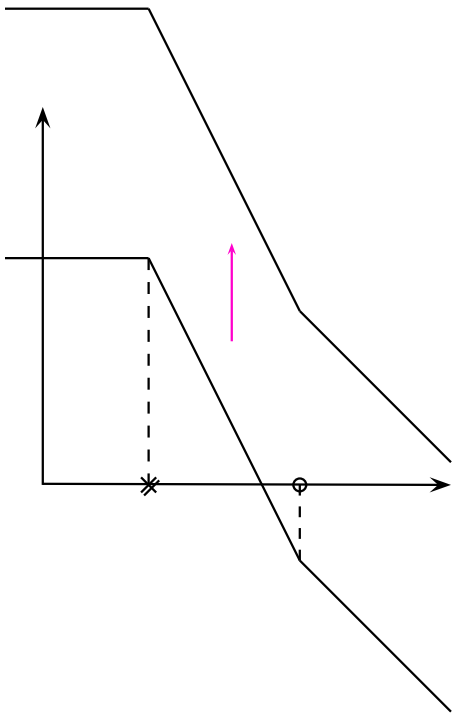
$$f_c = \frac{200\text{kHz}}{6} = 33\text{kHz}$$

we can accept that crossover frequency goes **below** this value, but we **can not accept** that it goes **above** this value. Our design will consider this fact!

In the worst case possible, our system must work at most at 33 kHz!

Now, which is the worst case? Well, it depends on the converter and working mode we are considering!

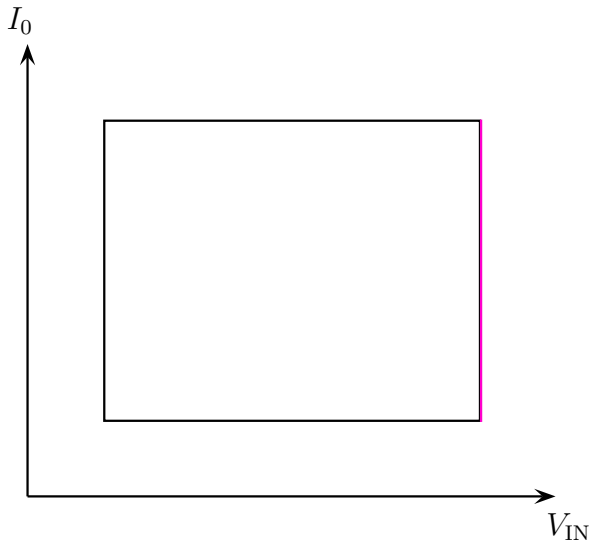
- For buck converter CCM (and all the circuits deriving from buck converter), we have a transfer function like this:



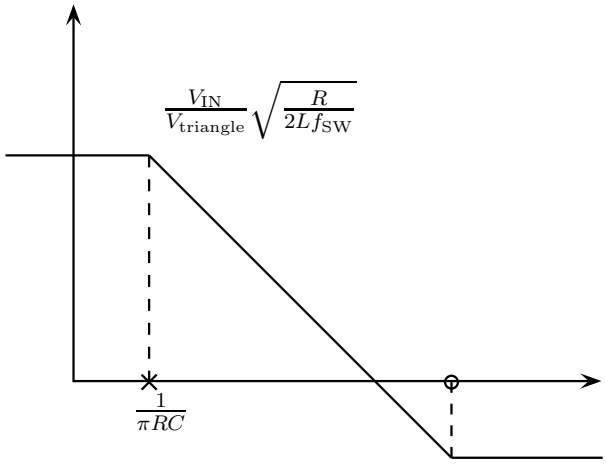
we have that

$$G_{\text{buck,CCM}} = \frac{v_{\text{IN}}}{V_{\text{triangle}}}$$

we have two fixed conjugate poles, and a fixed ESR zero: load does not change this graph (not the asymptotic graph: it changes the damping factor of the conjugate poles), but the input voltage yes! We change the multiplicative factor, so in Bode plot we are translating up and down our graph. The worst case, the one for whom we have the highest crossover frequency, will surely be the one with **highest input voltage value**. This means that the critical condition is this:



- For buck-boost DCM we have a transfer function like this one:



we have to consider the maximum input voltage (same reason of before), and the **minimum** load resistance R: if we increase R of a factor of 2 (for example), the gain increases of $\sqrt{2}$, and the frequency of the pole is halved; we have that the frequency of the zero is fixed (because it is relative to the ESR), so the crossover frequency will increase: the worst case here is relative to highest input voltage, lowest load resistance.

2.5 Measuring the loop gain

2.5.1 Introduction

We have to check that everything works: we know how to design all our stuff, but now we also have to verify that it works. There are many elements we don't consider, with our formulae, for example the presence of isolators in the loop, which make worse our loop gain. The goal of this section is to show how to measure the loop gain. We are going to introduce some methods, working for almost each closed-loop system. There are two kinds of methods:

- indirect measurements: we measure something which depends on the loop gain T, and so find a relation with T and evaluate it;
- direct measurements: we measure directly the loop gain.

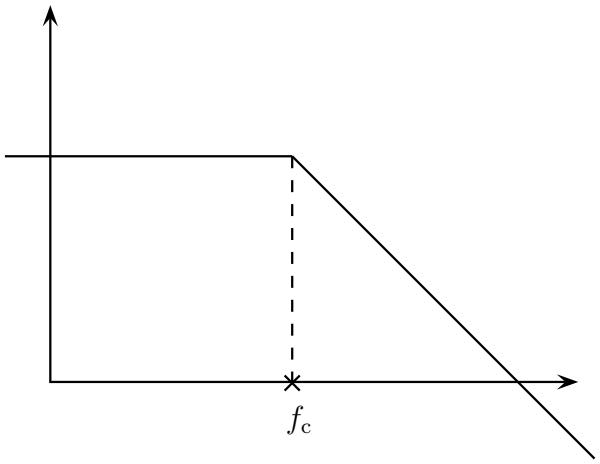
There are many indirect measurement techniques: time domain, frequency domain, etcetera; in time domain what we can measure is the output voltage, as a function of the input voltage:

$$v_0(t) = f(v_{\text{in}}(t))$$

In frequency domain, we can measure the transfer function of the system:

$$\frac{V_0(s)}{V_{\text{in}}(s)}$$

and also the output impedance, which is $Z_0(s)$; these are examples of indirect techniques. All these techniques are used often in amplifiers; we can have, for example, something like this (for an amplifier):



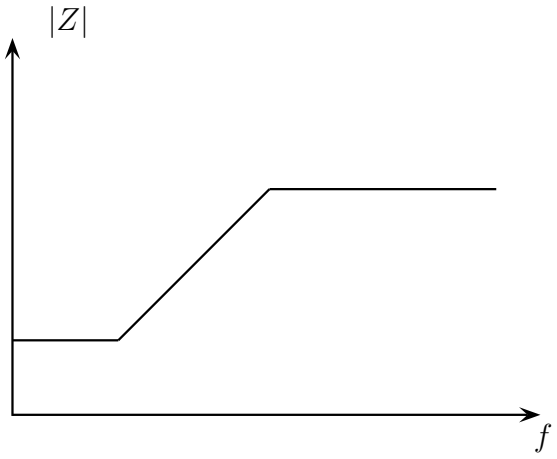
Above the crossover frequency f_c an amplifier does not work as an amplifier: it does *what it can do*; before f_c, we are almost sure that it will work as an amplifier.

Using these techniques on a power supply is not so easy: as input we have a reference voltage, which is not an actual input! This means that we don't have an actual input:

$$A_F = A_I \frac{T}{1+T} + A_0 \frac{1}{1+T}$$

the second term is usually neglected; the first term is multiplied for this function of T, which is called **discrepancy factor**: usually the discrepancy factor is almost equal to 1 (if the loop gain is high enough).

The output impedance behaves like this:



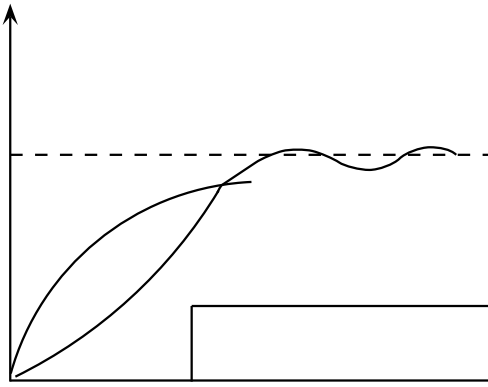
In some cases we have something like this behaviour: the frequency behaviour of an amplifier! If Z goes up with frequency we have an inductive

behaviour; this is just a model, because usually we don't have inductors (it may happen, but this is not what we want to explain); if we remember the Blackman's formula, we have that:

$$Z_{0F} = Z_{0D}\frac{1 + T_{SC}}{1 + T_{OC}}$$

in general, if we have an output voltage, T_{SC} is zero, because we are short-circuiting a voltage to ground, and we have just the denominator term; if we increase the frequency, the effects of the feedback decrease, so T_{OC} goes down, and we increase Z: this is just a feedback effect, not an inductive effect.

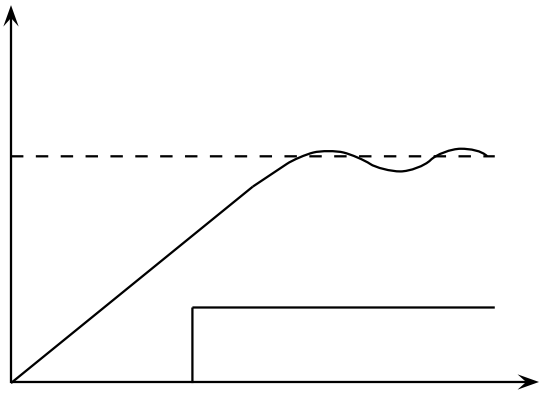
For power supplies a time domain approach can be a little bit better: in time domain we can use as input a step, and get a behaviour like one of these two:



Observing these waveforms for example in a scope, gives us some informations about the type of this system. Given the time constant of the system τ, we have that

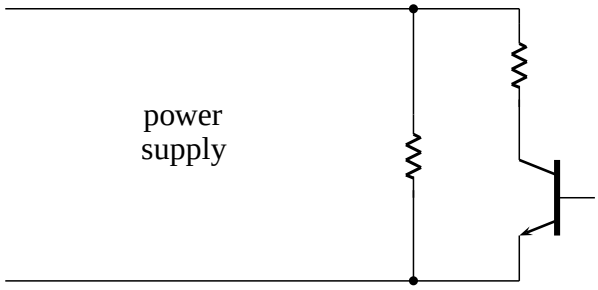
$$\tau = \frac{1}{2\pi f_c}$$

If we have an exponential transient, we have (with very high probability) a first order system (2); if we have some ringing (1), we have a second order system. By measuring the final value we can evaluate the DC gain, and by watching to the shape we can identify the system type: with a first order system we are sure to have a very large phase margin, and with a second order type system a worse phase margin. From an amplifier we can also have responses like this one:

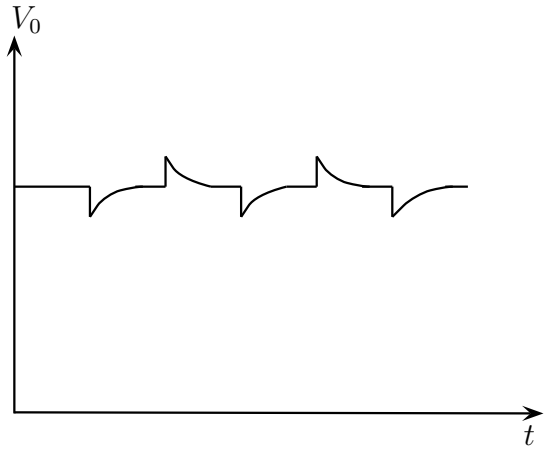


We can have a straight line, and then ringing: this shows the slew rate limitations of our system.

Again, problem: we still don't have input, in a power supply, so the idea is good, but not for a power supply: we have an input, but we can not remove it! What we can do for some power converters is to study the variations of the output voltage depending changes of the load; an idea is to use a system like this one:



by changing the current on the transistor, we can change the load, making it lighter or heavier. For example, from an analysis like this one, we can obtain something like this:



what we can know, from this system?

- we have a first order system (because we have exponential transients), and

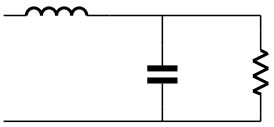
$$\tau = \frac{1}{2\pi f_c}$$

- we go back to the exact steady state value: we have **no DC error**, so this system is **type 1**; these system have very high DC gain: there is an integrative behaviour, a pole in the origin[2];

- the step before the exponential is not under the closed loop control: the loop can work at low frequencies (the maximum frequency is the crossover one, f_c), so this first response is an open loop response. The amplitude of the step is basically given by the output capacitor ESR R_S:

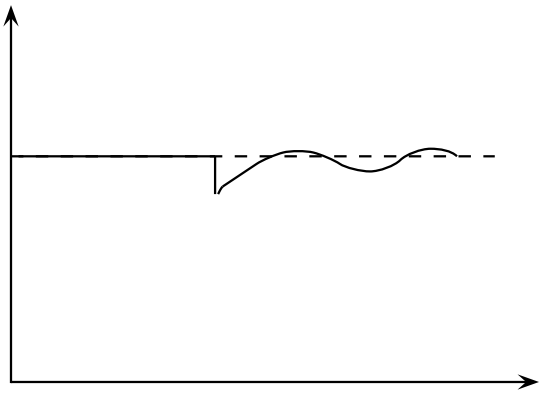
$$\Delta v_0 \sim \Delta i R_S$$

In a buck converter, for example, we have something like this:



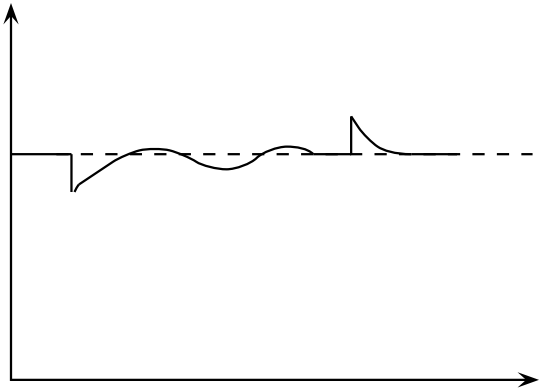
the inductor introduces an inertia, because it limits the speed of the change, so for a small time we can say that the inductor behaves as a constant current source. This means that the extra current coming through the load, through the switch (when it is closed), can not come from the inductor, due to its inertia. The extra current comes from the capacitor, so we have a voltage drop through the capacitor's ESR, and this is what we see in the output. If our system is type 1, we have that, after a transient, everything goes back to the steady state. If our design is not so good, and we have a small phase margin, we have something like this:

[2]Let's remember that pole in zero means infinite gain, means to have a capacitor connected to an infinite resistance, and in real world does not exist anything like this!



oscillations can also continue, don't be damped.

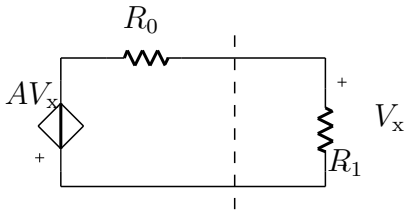
In some cases, typically in buck converter (which has a very low phase margin), we can have something like this:



We can have two different behaviours, depending on the fact that we add or subtract load: two different responses! Why? Well, because, if we are making the load too light, we go from CCM to DCM, and we know that DCM behaviour is a 1-pole behaviour.

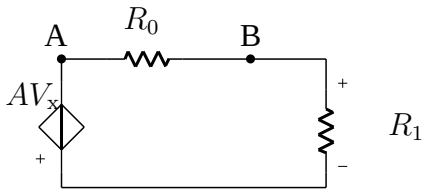
2.5.2 Direct measurement

Let's start this subsection with a question: what is the loop gain T? Well, **any** closed loop system can be modelled like this one:



we can put a controlled source, which may have a certain resistance R_0, and a load, R_1: the controlled source is driven by the V_x voltage on the R_1 load, so we change the input voltage by changing the output voltage. This is a general representation of any closed loop system.

Using this representation, we can introduce a test voltage V_T instead of the controlled source, evaluate V_x, and see that:



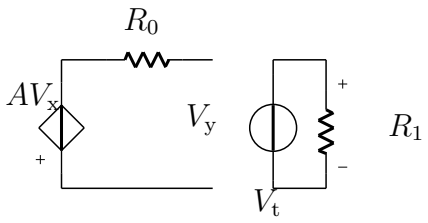
$$V_x = V_T \frac{R_1}{R_1 + R_0}$$

so, if we re-substitute V_T and AV_x, we obtain that:

$$T_{real} = A \frac{R_1}{R_1 + R_0}$$

This, for our theoretical calculations: this is the actual value of the loop gain, but we can not measure it so easily: the A node is not available for us: we need a way to measure the loop gain (even with some approximation).

What can we do? Well, the only available node is the B node: it can be, for example, the output node (this may be any node of the circuit, if it satisfies some criteria that we are going to introduce soon); what happens if we **cut** at this point? Well, something like this:



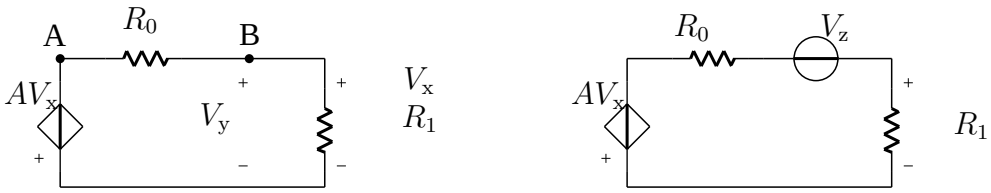
If we are very naive, we can put a test generator V_T in the output node, study V_x and see what comes back; we can see that:

$$T_1 = -\frac{V_y}{V_x} = -(-A)\frac{V_x}{V_x} = A$$

this T_1 is very different from T_{real}, unless a case: if we have that: $R_0 \sim 0$, so $R_0 \ll R_1$, we have that $T_1 \sim T_{real}$. This method can not be used in

electrical/electronic engineering: it works maybe in some steam engines, but it does not work here: in electronics we always have very high loop gains, so if we open a loop, we don't have time to put the stimulus: the system will saturate in a while.

We need another way: let's consider this modified circuit:



If we assume that we cut for a very short time the circuit, put a V_x and a V_y voltage source (which model the presence of those voltages). Now, we can add a V_z generator, which is:

$$V_z = V_y - V_x$$

In these conditions, the circuit is not changing. Now, the circuit is at an **open loop** circuit: now, with this trick, V_x is not controlling the source, so we lose the feedback. So, now, if we remove V_x, we have that:

$$-\frac{V_y}{V_x} = T_2$$

This is another loop gain evaluation. In this condition, our system is **closed loop**: we have no saturation. What we have to do is to insert a voltage source V_z in series to the loop, so, given the voltages V_y and V_x, we will have that their ratio is something close to the loop gain. Why just close? Well, let's see it: we have that

$$V_y = -AV_x - V_{R_0} = -AV_x - R_0\frac{V_x}{R_1} =$$

$$= -V_x\left(A + \frac{R_0}{R_1}\right)$$

so:

$$T_2 = -\frac{V_y}{V_x} = A + \frac{R_0}{R_1}$$

Now: is $T_2 = T_{\text{real}}$? No: they may be close, but not equal! T_{real} is the **actual**, theoretical loop gain; T_2 is just an approximation, obtained from

a technique which can be used in some practical cases: it is intrinsically approximated, but it can be used without sending our system in saturation, or something else. There are some conditions which ensure that this method works; we can find them, simply by searching for conditions which ensure that:

$$A + \frac{R_0}{R_1} \sim A\frac{R_1}{R_1 + R_0}$$

this happens if:

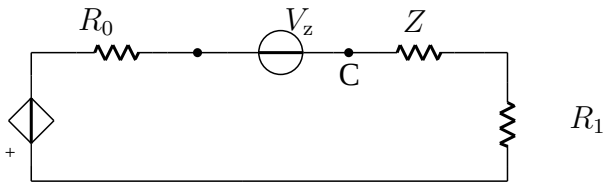
$$A \gg \frac{R_0}{R_1}$$

and

$$R_0 \ll R_1$$

both these conditions must be satisfied: we need a high A, and to introduce the V_z generator in a node with strong impedance mismatch. V_z must be small enough to not drive our system in saturation, but high enough to be observable.

A couple of considerations: when we are in lab, we have to use an actual voltage source, which will have an output impedance Z:



In this circuit, obviously, the C node is not available; if we re-do the calculations, we find that:

$$T_2 = -\frac{V_y}{V_x} = A + \frac{R_0}{R_1}$$

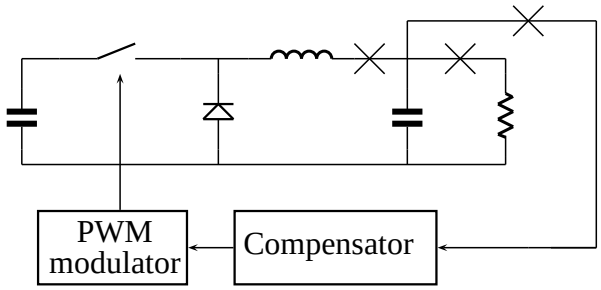
so, it does not have any effect; the **actual** value of T is:

$$T_{\text{real,Z}} = A\frac{R_1}{R_1 + R_0 + Z}$$

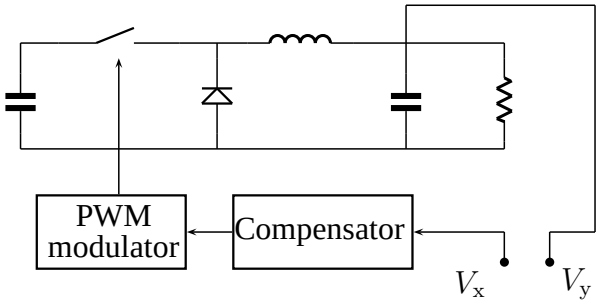
our loop gain goes down, so what we measure (by using the **practical** method) does not take account of Z; our loop gain is basically decreased, so our system will be more stable.

2.5.3 Practical use of this technique

How can we do it in real world? How can we **measure**, with instruments, the loop gain? Well, let's consider a circuit like this:



The first question is: where can we cut? Well, basically, where there is a strong impedance mismatch; the best point is the cut of the feedback: we have to find a point where information is brought by voltage amplitude (not by duty cycle, like happens in the inductance); a good point can be the output point, with output impedance which is far smaller than the load impedance, but this is a point with strong current: it is bad to put a strong current on it; the best point is the feedback: analog signal, strong mismatch, low DC current. We have that:



$$-\frac{V_y}{V_x} \sim A$$

and A is the loop gain: this is higher than 1! It happens that $V_x \sim 0$ (is very small), and V_y goes up and down, just to counteract the effects of V_z: to cancel what V_z is injecting. The switch mode output voltage, which equals V_y, will be almost constant, thanks to the fact that this is a controlled system.

This is a **linear system**, and we are measuring a gain of a linear system: we don't expect to have dependence on V_z, because, if a system is linear, its

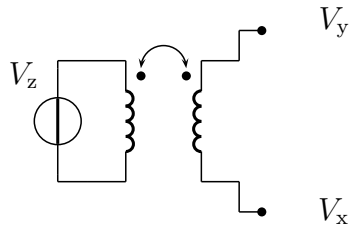
gain is constant respect to the input (output to input characteristic is a line), so all ok!

At this point, we still have two practical problems:

- how to inject the V_z signal;
- how to measure T, in magnitude and phase.

First of all: which waveform have we to use for V_z? Basically, sinusoidal waveforms: we want to measure a transfer function, so use a monochromatic signal is the best choice. There are four ways to inject signals, and we are going to explain them all.

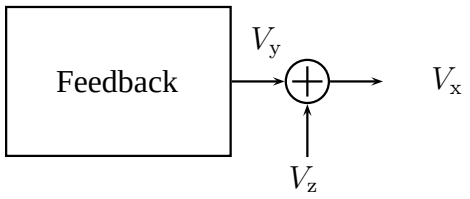
1. We have a signal, which derives from a waveform generator; usually, those generator have an output which is **grounded**: we have to face this problem. The idea we can have is to use a **transformer**, putting in one node V_z, obtaining, in the other side, V_y and V_x:



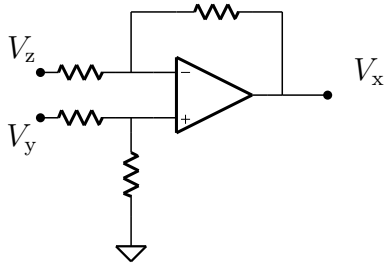
   This transformer has to be a wide-band transformer: we want to find the phase margin, the crossover frequency, and it can be go up to 10 kHz or something similar. This is not a standard 50 Hz transformer! One available transformer in lab can be the passive current probe. The probe is basically composed by a clamp which has, inside it, a ferromagnetic material with a certain number of coils we put around it, in order to measure the current (some kind of half-transformer). Transformers are reciprocal, so if we want to use a current probe as an injector, we have to take the probe, remove the BNC box, and go directly to the signal generator, by connecting a wire to the other side of the ferromagnetic material, creating a kind of transformer.

   This system has a drawback: we have a high number of coils, so if we put in the transformer 1 V, out of it we have something similar to 2 mV: this transformer injects a very low voltage into our system. Can we change the ratio? Well, we may turn the wire, connected to the other side of the material, more times than 1 (3 o 4 times), in order to increase the ratio.

2. Another way to do it is injecting V_z using an adder:



   We just add a node which permits to add the V_z signal to the feedback loop, in the point where we want to *cut*. How to implement an adder? Well, we can use this simple op-amp circuit:



   We don't have to care about the − input: even if it is an inverting adder, we are just considering a sinusoidal signal, so we are inverting the signal we add, and this is not important! This system can go down to 0 frequency, but it costs an op-amp: we have to put it just on the prototype of our system, not in production.

3. Design a transformer using op-amps (crazy thing!).

4. Use an isolated signal generator, which is large, very expensive, so we are not considering it.

So, once we injected this voltage, we have to measure, in some ways, the ratio between V_y and V_x; here, there are the main methods we can use.

1. By using a scope: we can use two probes, and measure the phase difference and the ratio of the amplitudes; this is easy, cheap, and we can use the instruments available in lab. Another note: if we are looking for the crossover frequency, we just have to change the frequency of the signal V_z, until the ratio of the two amplitudes become 1. At this condition, the phase shift between the two signal equals the phase margin φ:

$$\varphi = \angle T - 180^\circ$$

so, remembering that:

$$\angle T = \angle \left(-\frac{V_\mathrm{y}}{V_\mathrm{x}} \right)$$

we have that the phase of T already has a phase shift of -180°; so:

$$\angle \left(\frac{V_\mathrm{y}}{V_\mathrm{x}} \right) - 180^\circ - 180^\circ = \angle \left(\frac{V_\mathrm{y}}{V_\mathrm{x}} \right)$$

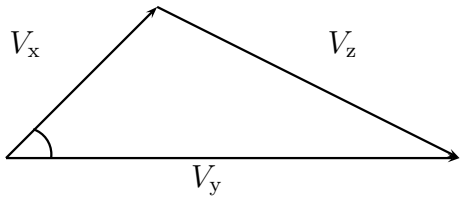
2. By using a low frequency network analyzer; this is just an instrument with three connectors (it is quite different from the more common RF network analyzer), 1 output, 2 inputs A and B. This instrument can directly give us

$$\left| \frac{V_\mathrm{A}}{V_\mathrm{B}} \right| \quad \text{and} \quad \angle \left(\frac{V_\mathrm{A}}{V_\mathrm{B}} \right)$$

This is very very easy to use, but quite expensive; for Power Electronics there are cheaper network analyzers.

3. By using a vector voltmeter (which is simply half of the previous instrument).

4. By using a scalar voltmeter (which can just measure amplitude, but not phase). With it we can measure V_x, V_y, V_z; a note: if we remember that



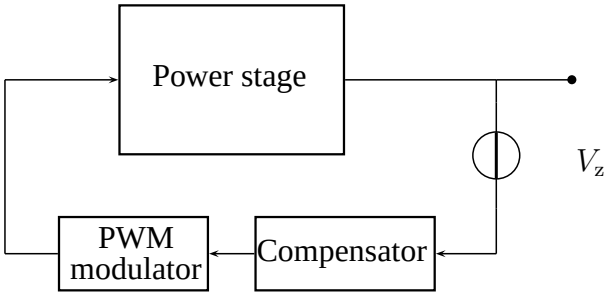
we can use the Carnot theorem (cosine theorem) and find the angle between V_x and V_y, remembering that

$$V_\mathrm{y} + V_\mathrm{z} = V_\mathrm{x}$$

2.6 Alternative control modes

2.6.1 Introduction - feedforward

From the theory we studied, we know that we can measure the loop gain with something like this:

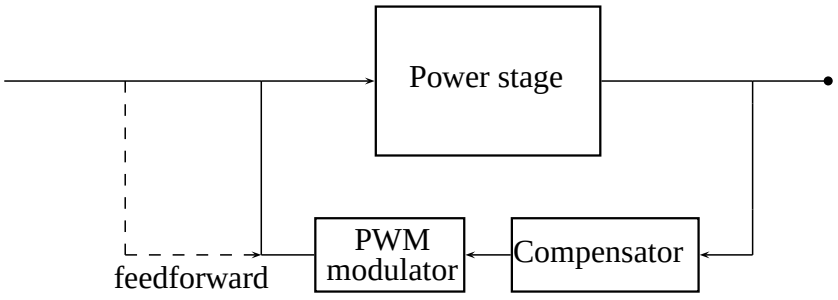


We know that:

$$-\frac{V_y}{V_x} = T$$

but, with this configuration, we can also do other measurements! For example, let's consider the ratio of V_y and V_x: this is what we have out of the compensator, on what we have in the compensator: the **compensator gain**.

Why are we talking about this? Well, we want to emphasize one fact: the method we used to control our converter is **voltage mode**: we measured the output voltage, and changed d. There are also other methods, borrowed from control theory: we know that output voltage changes, because also input voltage has some variations: what we can do is to measure **also** the actual V_{IN}, and give it directly to the PWM modulator: we sneak the input voltage, send it directly to the PWM modulator, without using the feedback: in this case, our control becomes faster, because we don't pass through the compensator. This technique is called **feedforward**:



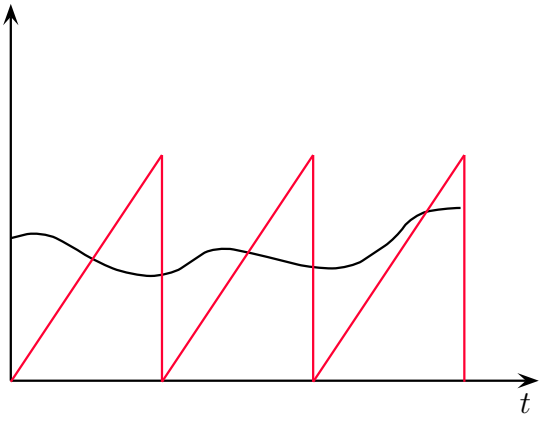
Let's use an example, in order to understand it better: in a buck converter, we have that:

$$V_0 = V_{\text{IN}} D$$

So, with the feedforward, if V_{IN} increases for some reasons, the control has to decrease immediately the duty cycle:

$$D \propto \frac{1}{V_{\text{IN}}}$$

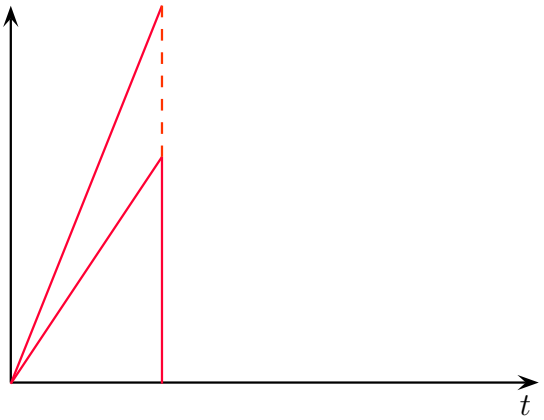
We have seen that the duty cycle can be generated as:



Now, the duty cycle must not be generated from the error signal; we know that:

$$D = \frac{V_{\text{error}}}{V_{\text{triangle}}}$$

If V_{IN} increases, what I have to do in order to decrease D is to increase V_{triangle}; an easy way to do it is to make the slope of the triangle be proportional to V_{IN}:

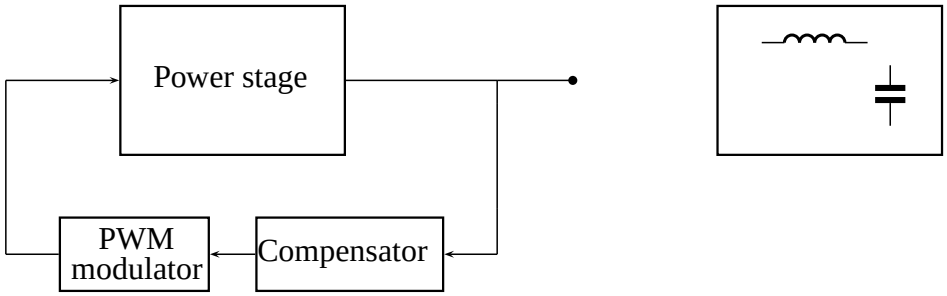


we change the slope, but keep constant the period.

Let's remark that feedforward must be **added** to the feedback: we **have to** measure the output voltage, all the times!

2.6.2 Current mode

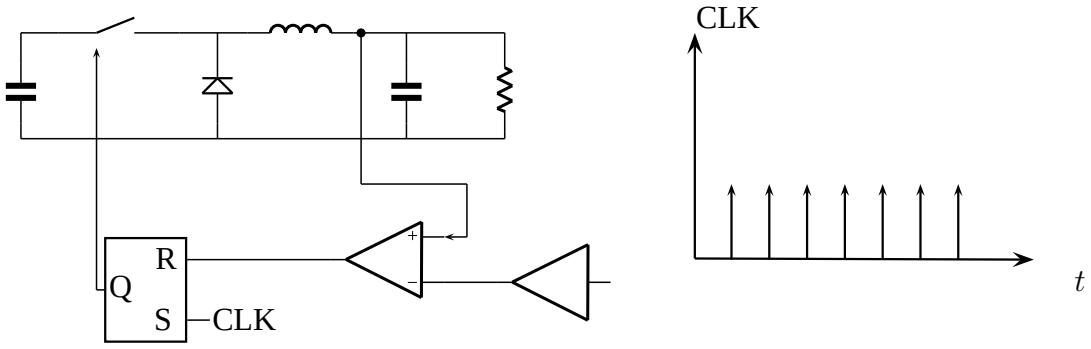
There are also other solutions, for the control problem. As we know, inside the power stage, we can have something like this:



What we can do is measure also the state variables of the system: if we measure **all** the state variables, so, the already known v_0 and i_L, we can increase the performances of the control. If we measure i_L we obtain the so-called **current mode**; it is defined with these four steps:

1. as it begins a new cycle, we turn the switch on;
2. we **wait** until i_L reaches the desired value;
3. we turn the switch off (we open the switch);
4. the inductor current, when the switch is off, starts to decrease, and we **wait** the beginning of the next cycle.

Let's study for example a buck converter:

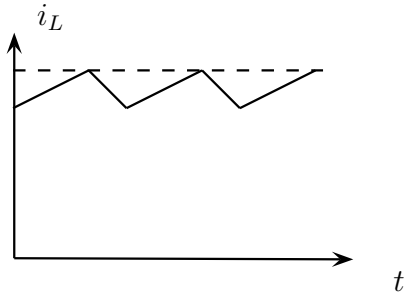


We measure the inductor current, and obtain a voltage proportional to i_L, with a resistance factor R_S (just a conversion factor from i_L to v_L. We introduce a S-R flip-flop, and its output goes to control the switch. To the *set* input we introduce a clock, which is composed by a sequence of pulses; we connect it to the set, just because each pulse corresponds to the begin of a new cycle. Then, we have to wait that i_L reaches the desired value, v_L with it, and we have to compare this v_L voltage with a comparator; the other input of the comparator is V_{control}, which is the voltage which is compared with the v_L voltage: it is the output of an error amplifier, which compares the output voltage of the power supply to a reference voltage. V_{control} establishes the maximum value of the inductor current we admit: it chooses the **desired value**.

This system has two loops: a current loop, and a voltage loop.

- The current loop has no poles, no filters of any type, so it is a **fast** loop. As soon as i_L reaches the control value, the desired value, in the next cycle we have that the voltage comparator resets the flip flop, so all reacts promptly. This is a non-linear loop, because we have non-linear elements, like the flip-flop.
- The voltage loop senses the output voltage and changes the compared voltage. It is an analog loop: it has an error amplifier (which is an analog amplifier), and it is slow, because the error amplifier is based on a compensator, which has poles.

Let's do some calculations, in order to design this compensator. We know that:



We have to compare i_L, represented as a voltage; if we are using a buck converter, we have that:

$$\overline{i_L} = I_0$$

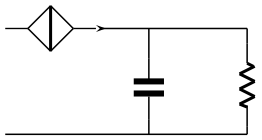
More in general, we have that, if our loop is fast enough:

$$\overline{i_L} \sim i_{L,\text{peak}} \triangleq i_{\text{peak}}$$

This, because, if everything happens in a small time, we have small current changes! For this case:

$$\overline{i_L} = I_0 \sim i_{\text{peak}} = \frac{V_{\text{control}}}{R_{\text{S}}}$$

where i_{peak} is the controlled value. We obtain that the inductance behaves as a controlled current source, and its value is $\frac{V_{\text{control}}}{R_{\text{S}}}$.



Let's find the transfer function:

$$\frac{V_0}{V_{\text{control}}}$$

Well, calling Z the impedance seen by the current generator, we have that:

$$V_0 = Z\overline{i_L} = Z\frac{V_{\text{control}}}{R_{\text{S}}}$$

where

$$Z = R \oplus \frac{1}{sC}$$

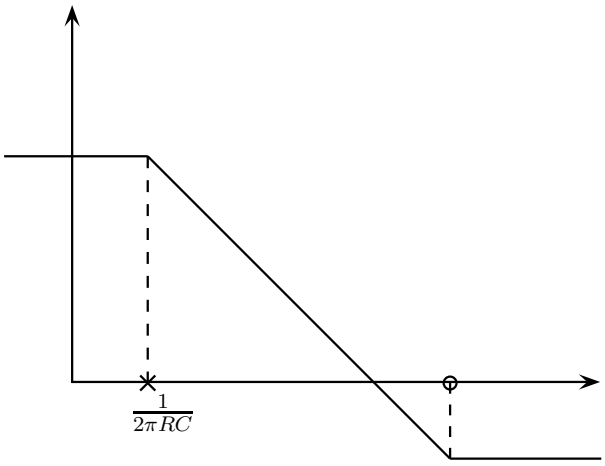
so

$$\frac{V_0}{V_{\text{control}}} = \frac{R}{R_{\text{S}}}\frac{1}{1+sRC}$$

we have a DC gain, and a pole; if we want to be precise, there is also the usual ESR zero:

$$\frac{V_0}{V_{\text{control}}} = \frac{R}{R_{\text{S}}}\frac{1+sCR_{\text{ESR}}}{1+s(R+R_{\text{ESR}})C}$$

So, we have that the DC gain and the pole are moving, variable, and the zero is fixed:



So, let's see which are the advantages of this technique.

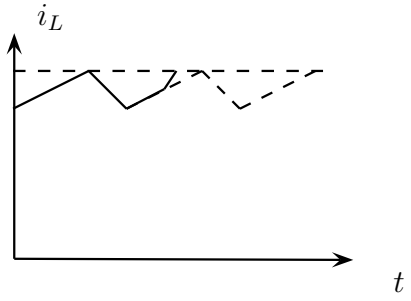
- We have no V_{IN} over there: this means that the audio susceptibility, the dependence of the system on the input voltage is almost null! This means that we don't need to introduce feedforward, because it is already implemented!
- We are missing one pole, because we are forcing the inductor to act as a current source: we have just a 1-pole dynamics, and we may use just a type-2 compensator, which is faster than the type-3 compensator.
- If load changes, if the load R decreases, the pole shifts to right, but gain decreases of the same factor: frequency and gain move together, and with the same factor. What happens is that the high frequency behaviour does not change with R, with the load resistance, because the crossover frequency does not change: the low frequency behaviour depends on R, but the high frequency behaviour no!
- If we keep increasing R, accidentally our system may move to DCM, and this model is no longer valid; there is an advantage respect to voltage mode: in DCM we have 1 pole (with different frequency) and 1 zero, so our compensator will not be totally wrong: the circuit is the same, with different values!
- If we have that load becomes a short circuit, the error amplifier wants to increase the voltage, and reaches the maximum; output will be limited in voltage! We can limit the control voltage with a zener diode, and prevent that ask of current for the loop: even if we have a short circuit, the output current can be limited, and the converter still survives.

With a voltage mode controller, if the load becomes a short circuit, the converter asks for the maximum voltage, we have $D = 100\%$, and current continues to increasing, destroying the circuit.

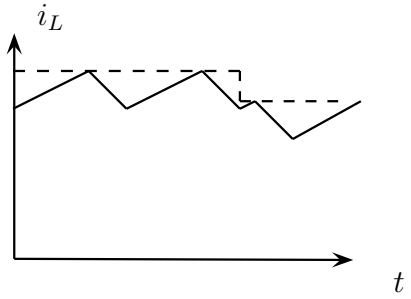
A check: if we increase the input voltage, it happens that

$$\frac{V_{\text{IN}} - V_0}{L}$$

increases! So, the ramp gets steeper, immediately! But this will adapt **immediately** our duty cycle, making close to zero the audio susceptibility: the slope changes immediately, without need to pass through poles or filters!



Another observation: if we decrease the control voltage, what do we have? Well, something like this:



It happens that the inductor current come down just in one cycle, the average current come down, and this in a very short time: we just have to wait the begin of the new cycle.

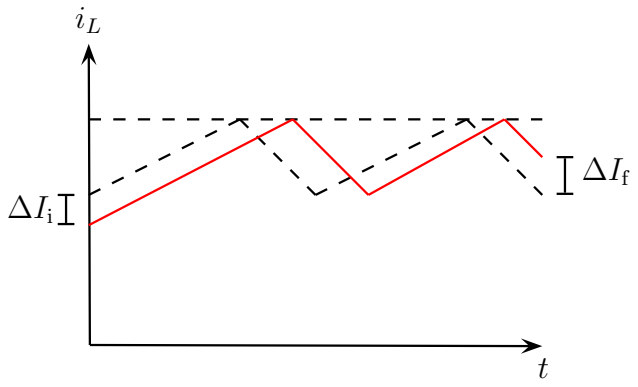
Current mode has also bad news, disadvantages.

- Money: we need some extra devices, so we have to spend more money! We have to measure i_L (with a resistor, or something else); the expensive element is the **current measure**, not the other elements!

- If we have some noise on the current i_L, immediately the comparator may sense it, and open the switch; the next cycle, we will recover the situation, but we have a very high noise sensitivity.

- If we increase V_{IN}, we have that $\overline{i_L}$, actually, changes; this means that we lose the approximation $\overline{i_L} \sim i_{\text{peak}}$, and we have to re-do the calculations! The fact that we lose this approximation, is the reason of the non-zero audio-susceptibility: average current errors!

- The most important error is related to the fact that if, during steady state condition, a noise signal stops our cycle, we have something like this:



  next cycle we try to recover; when it starts, we see that, at the end of the cycle, we may have a change of the current. Depending on the amplitude of this final Δ current, we may introduce an instability: if every time we have that this difference of current increases, we basically introduce instability! This type of instability is called **subharmonic instability**, because its frequency is one half of the switching frequency. This behaviour, so the fact that we generate harmonics under the fundamental, is a characteristic of some dynamic systems. After the first period doubling, period continues to doubling, so the frequency of the sub-harmonics continue to decrease, and the system tends to become chaotic.

  We want to avoid this situation, so we want to try to find a condition for whom this period goes to 0. Let's analyze 1 cycle (in the previous plot), and see what happens; we want that, for each cycle:

$$\left|\frac{\Delta I_{\text{f}}}{\Delta I_{\text{i}}}\right| < 1$$

Let's consider the two slopes of the two curves:

$$m_1 = \frac{V_{\text{IN}} - V_0}{L}$$

$$m_2 = -\frac{V_0}{L}$$

geometrically, we can write that:

$$\Delta t = \frac{\Delta I_{\text{i}}}{m_1}$$

$$\Delta I_{\text{f}} = \Delta t m_2$$

so, by combining the two, we obtain:

$$\Delta I_{\text{f}} = \frac{m_2}{m_1} \Delta I_{\text{i}}$$

so

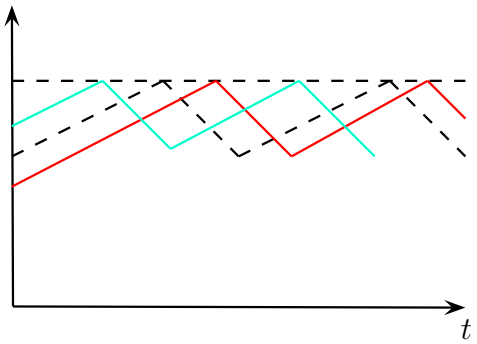
$$\frac{\Delta I_{\text{f}}}{\Delta I_{\text{i}}} = \frac{m_2}{m_1}$$

this is the condition which permits to damp out error; this can be written simply as:

$$D < 0.5$$

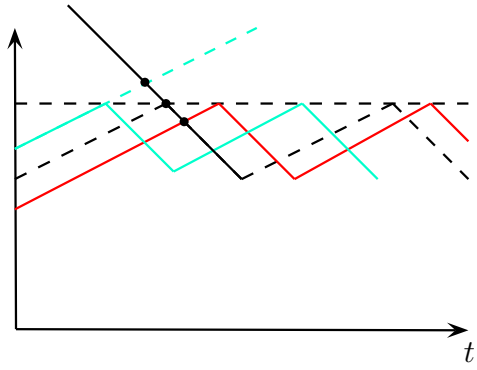
So, if we want to avoid subharmonic instability, we have to work all the times with $D < 0,5$.

We want to use converters also with $D > 0.5$, but it could be a problem; let's consider the three possible scenarios:

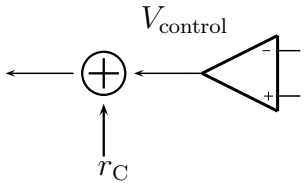


With the curve 1, all is ok; in the case 2, we have that ON time ends too early, so we have to delay the T_{SW} of a little time; about the case 3, we have to anticipate the T_{OFF} time.

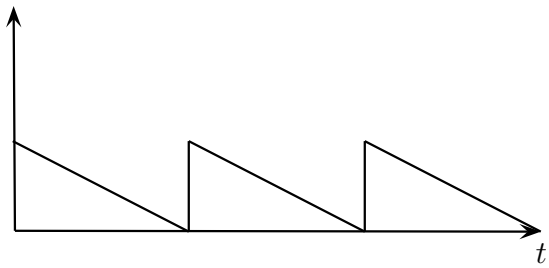
If we are able to solve all these situations, we can remove this error in just 1 cycle. How to do it? Well, let's study this graph:



But there is a problem: here, it seems that we know, at the beginning of the cycle, that there is some delay; this is absurd: when we start the cycle, we can't know if we will have errors; what we need, so, is a solution which is valid for any initial value, any initial condition. What we can see from the previous plot is that all the stop points are aligned on the same straight line: basing on this observation, we have to introduce a dynamic correction of the error, by changing dynamically the threshold; this means that we need a variable V_{control}, and in order to do it we have to add a **compensation ramp** (or **compensation slope**). Let's see this schematic:



Instead of having a constant voltage out of the error amplifier, so before the comparator, we ask for a variable control voltage, obtaining something like this:



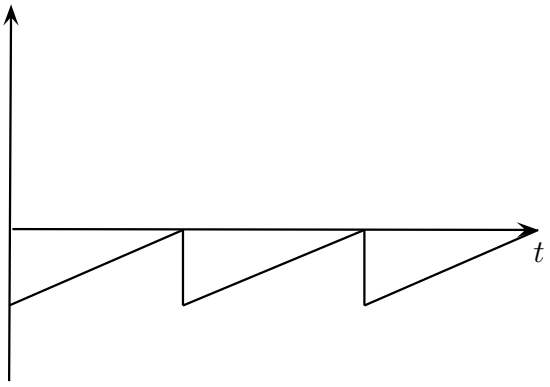
A descending voltage. The voltage comparator just compares this new voltage, given by the constant V_{control} plus the control ramp r_{C} with the v_L one:

$$i_L R_S <? > V_{\text{control}} + r_{\text{C}}$$

we can write that:

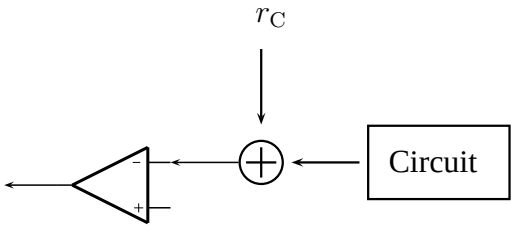
$$i_L R_S - r_{\text{C}} <? > V_{\text{control}}$$

so, the $-r_{\text{C}}$ will have this behaviour:



This means that this compensation ramp has this behaviour, this waveform, once we change its sign.

Let's remember that the compensator, the error amplifier, is basically an integrator: out of the integrator we can have any voltage we want, without changing its input: just for the initial conditions. Instead of this compensation ramp, if we put this one, the shifted one, we obtain an offset: a negative offset. This offset is included by the error amplifier: as said, the integrator can have at its output any DC voltage which is convenient for the loop. When we have in the circuit this offset voltage, we can refer it to the input of the compensator, simply by dividing it for the DC gain of the integrator, but it is almost infinite!



We can take the voltage, change the sign. Then, instead of adding my reversed compensation ramp, I add the compensation ramp, with its sign, in the other side of the compensator: simply, we have to add a DC voltage, in order to obtain a ramp out of it. Use this method is easier, because those ramps are easier to generate.

Which is the slope of this ramp, in order to remove, in one cycle, any possible error? Well, it is the maximum slope we can have: we have to add this voltage ramp on the other, and this means to delay or anticipate the time; if we want to have the maximum swing, this voltage must be

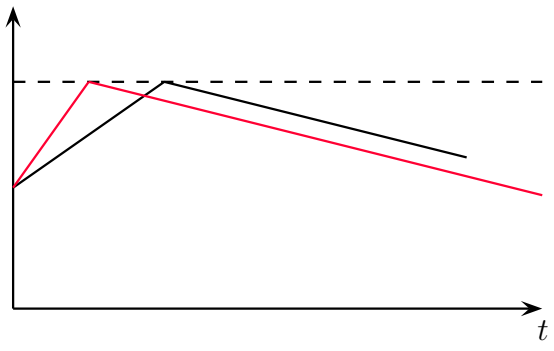
$$-\frac{V_0}{L}$$

This because all these points are aligned on this slope! The ramp slope we have to add, so, is just this! Actually, we forgot something: we have still to have a resistor term (R_S), in order to obtain a voltage slope (over time):

$$-\frac{V_0}{L}R_S$$

Now: what happens if our compensation ramp is not the right one? No problem: instead of removing in one cycle our error, we reduce it; this means that we introduce the condition which removes the sub-harmonic instability, so in some cycles it will go ok!

This is not the only compensation ramp we can use: we can use a compensation ramp to solve another problem: up to now we are controlling **peak current** (our current mode is based just on the control of the peak current); if we increase the voltage V_{IN}, the ramp goes up steeper, but goes down with the same slope (because V_0, which determines the value of the descending slope, is always the same).



We used, as hypothesis, the fact that the peak value equals the average value; this is not true at all, and the difference between $\overline{i_L}$ and i_{peak} changes

with the bias point (because, actually, audio susceptibility is not zero); this goes to destroy the approximation of the fact that we have just one pole. If we really want to use this approximation, we have to introduce another slope. We know that:

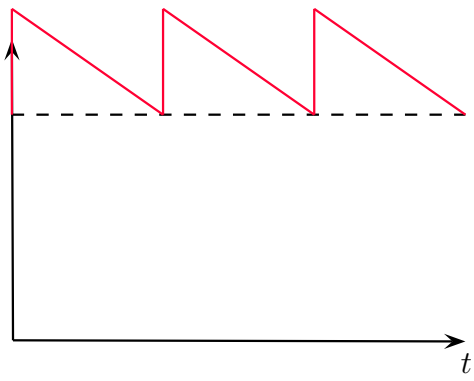
$$\overline{i_L} = i_{\text{peak}} - \frac{1}{2}\frac{V_0}{L}\frac{1-D}{f_{\text{SW}}}$$

(we have found this equation simply by taking the peak current, and using the ramp down expression; then, we averaged with the Nutella theorem).

This is the actual value of $\overline{i_L}$: i_{peak} is what we can control, and the other part is the error, which depends on the duty cycle D; this is a problem: we don't know the exact initial conditions, so input and output voltage, and so D! We don't know the initial conditions, so the initial D, and this is a problem: we can not correct *a priori*. What we know is that, if $D \sim 1$, our correction to the term must be very small; if $D \sim 0$, it will be something like

$$+\frac{1}{2}\frac{V_0}{L}\frac{1}{f_{\text{SW}}}$$

So, we have to be ready for every value of D! We have to find something like before:



This correction depends linearly on the duty cycle; if we add on the top of the control voltage this term, which changes in time, we do something similar than before: we add another compensation ramp; with this idea, we obtain that

$$\overline{i_L} = i_{\text{peak}}$$

The maximum correction we need is:

$$+\frac{1}{2}\frac{V_0}{Lf_{\text{SW}}}\frac{1}{T_{\text{SW}}}$$

The T_{SW}^{-1} term, because we have to introduce this slope for a time equal to T_{SW}: this correction must go from 0 to T_{SW}, and we obtain:

$$+\frac{1}{2}\frac{V_0}{L}$$

This is the slope correction we need in order to remove our problem: with this, we remove the average error, so we move to (ideally) infinite frequency the second pole. There is one term missing:

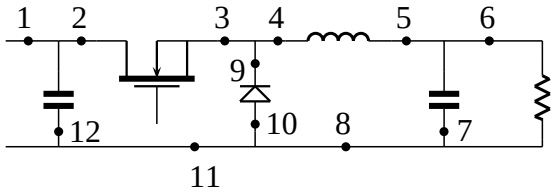
$$+\frac{1}{2}\frac{V_0}{L}R_{\mathrm{S}}$$

this R_{S} term permits us to handle voltages instead of currents.

Any compensation ramp with slope from this value to $\frac{V_0}{L}$ to this one is good!

2.6.3 How to measure current

Let's consider the usual buck converter:



we know that, in CCM:

$$V_0 = DV_{\mathrm{IN}}$$

The duty cycle D is the same in both current or voltage modes: no matters how we control the system! What changes, is how to measure it, but its actual value remains the same.

We are talking about current mode, so our purpose is to measure the inductor current. Which are the valid points to measure this current? Well, let's analyze them.

Node 1 is not good, because we don't have peak current here: just DC current; node 2 is ok, because, during T_{ON}, we have i_{peak}; same thing for 3, 4, 5. Nodes 6, 7, 10 and 12 are not ok, because there are missing the DC or the ripple values. What about the remaining nodes? Well, about node 9, it seems to be ok, but we have a problem: it conducts just during T_{OFF}, so we can't use it, because, when we close the switch, there is no current there: if we stay in point 9, we never see current, even if there is some through it. 8 and

11 are valid, but it is better to avoid them: this is not an isolated converter, so we expect that the GND (or chassis) is the same for load and input. If we connect those points, we short-circuit this current path, so current goes one part to one section, and one part to the other. This has another problem: the two GND points move, so current mode voltage across the load goes up and down, because we have the current sensors have a constant differential voltage, but a variable common mode voltage, and this makes our sensor be a transmitter.

So, 8 and 11 are not ok for EMC problems and because current measurements are not very good in those points.

So, what about the four good points? Well, let's classify them:

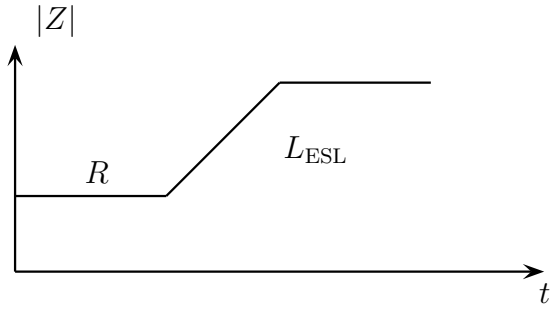
- about node 2, we have just **part** of i_L, and **constant voltage** (equal to V_{IN});
- about node 3, we have just **part** of i_L, and **variable voltage** (changing from 0 to V_{IN} at high frequency);
- about node 4, we have **full** i_L, and **variable voltage**;
- about node 5, we have **full** i_L, and **constant voltage**.

Now, before discuss which points are better than the others, let's introduce the two modes we can use to measure i_{peak}:

- with resistors;
- with current transformers.

Measurements with resistors

We are going to introduce how to measure current with resistors, and to discuss which points are the best. We know that a resistance can be modelled by using the Ohm's law:



$$R_{\mathrm{S}} = \frac{V_{R_{\mathrm{S}},\mathrm{max}}}{i_{\mathrm{peak,max}}}$$

$V_{R_{\mathrm{S}},\mathrm{max}}$ is a **practical constant**: it is defined by the manufacturer of the integrated controller, and it is about 1 V (or 1.1 V). i_{peak} is defined by the problem.

Usually, the value of R_{S} is out of the various standards (E12, E24...), so we have to choose higher or lower values. What do we use? Well, we **must** guarantee that we reach the maximum voltage value at the right point, not before the peak, so we have to use **lower** resistances, because we need to see the i_{peak} value.

How can we measure the dissipated power (the other important parameter of a resistance)? Well, we know that:

$$P_{\mathrm{diss}} = I_{\mathrm{RMS}}^2 R_{\mathrm{S}}$$

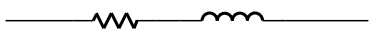
we are talking about dissipated power, so we need the RMS value; the resistance value is the **actual** one, not the nominal. So:

$$P_{\mathrm{diss}} = I_{\mathrm{RMS}}^2 R_{\mathrm{S,actual}}$$

So, which points must we use? Well, by a point of view, we prefer points 2 and 3, because they have less current, so they can decrease the dissipated power. If we have to choose between 2 and 3 for one set, and 4 and 5 for the other, which ones do we choose? Well, we have a floating resistor, so we prefer to choose, between 2 and 3, the section 2: it has a DC common mode voltage. Section 3 has a high frequency common mode voltage, so we have a square wave, with many frequencies, and it requires a higher CMRR to remove this problem. Same story for 4 and 5: we prefer, for the same reason, the section 5, because of its DC common mode voltage.

So, now we know that the two best sections are 2 and 5, and we have a good reason to use 2; 5 introduces more dissipated power, but it has less common mode DC, so, depending on what we need, also 5 can be used: each point has pro and con! If we have common mode limitations (due to our amplifiers), we have to use the section 5; if we have no CMRR limitations, we can use the 2, which guarantees higher η.

Resistors have another problem: they are not resistances, so they have parasitic elements disturbing their resistive behaviour. In particular, the model of a resistor may be this:

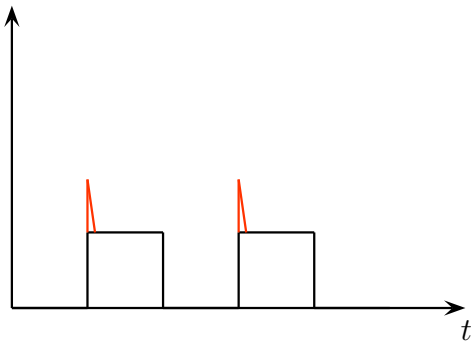


Very important in our model is the ESL (Equivalent Series Inductance), which introduces a zero at:

$$f_z = \frac{R}{2\pi L_{ESL}}$$

we are working with small resistance values, so f_z may be at very low frequencies!

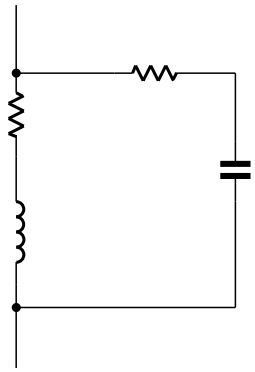
If we are working in section 2, with high $\frac{di}{dt}$, so we have something like this:



This is the effect of the ESL: this derivative of i goes into the inductance, and gives an extra voltage.

Current mode worked on the principle of: close the switch, and wait until we reach the peak current; this is bad, because our sense value can be influenced by the ESL, and by the high voltage produced by it, due to the high voltage derivative.

We have to cancel the impedance, by introducing a pole at the top of the zero; in order to do it, we just have to place an RC circuit like this:



Where we have to set:

$$\frac{L_{\text{ESL}}}{R_{\text{S}}} \sim RC$$

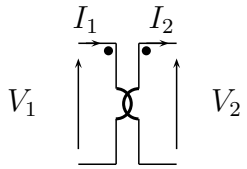
if we realize something like this, we obtain a wide-band current sensing system.

We don't do this very often, because it is done only in systems with very high current.

In modern ICs we can get rid of those extra spikes, with another trick: controllers know when the cycle has to begin, so we can add a blanking circuit which don't senses what happens at the begin of the cycle, ignoring the spike; using a blanking time of 50 ns or something similar, we can ignore this problem!

Some remarks about transformers

Another way to sense the current is based on current transformers. Let's introduce some remarks about transformers:



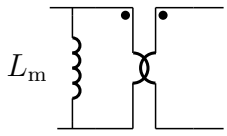
where

$$\begin{cases} V_2 = nV_1 \\ I_1 = nI_2 \end{cases}$$

if we multiply the two terms, we obtain that:

$$I_2V_2 = I_1V_1$$

This means that we have no losses, and no frequency limitations (with this **ideal** model). An **actual** transformer has frequency limitations: its model is something like this:



L_{m} is called **magnetizing inductance**: we would like that $L_{\text{m}} \to \infty$, in order to avoid those frequency limitations.

In a transformer, we have that the flux φ equals:

$$\varphi = \int_0^t v(t)\mathrm{d}t$$

when we put an input current, one part goes to the magnetizing inductance, and it generates flux (which risks to saturate the transformer), and the other part in the transformer, so in the other branch. There are two negative situations:

- if we put a small load, so a load which requires a high current (a heavy load), we risk to overload the transformer, damaging it, but avoiding saturation: Joule effect damages the transformer!
- if we have a current in the L_m which is too high, the transformer saturates, so stops to behave as a transformer!

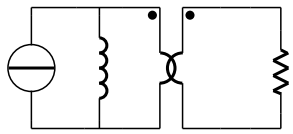
the current on the magnetized inductance i_m is:

$$i_\mathrm{m} = \frac{1}{L_\mathrm{m}} \int_0^t v(t)\mathrm{d}t$$

we want to keep i_m under the saturation limit. How can we avoid saturation in a magnetic component? Well, this integral has to be finite, so we have to **avoid DC values**: $V_{\mathrm{winding,DC}} = 0$.

Transformer as a current transformer

Given our simple model, if we put a current source on it, we have something like:



the load must be inserted, in order to give a path to this current. We want, ideally, that:

$$i_2 = \frac{i_\mathrm{IN}}{n}$$

this is not true: part of the input current will go through the magnetized inductance, so will not be transformed. We don't want large errors respect to the previous expression, so an idea is to have a very large inductance. We can say that:

$$i_{\mathrm{m}} = \frac{1}{L_{\mathrm{m}}} \int_0^t v_{\mathrm{primary}} \mathrm{d}t$$

in order to keep i_{m} small, we need a small voltage on the primary winding.

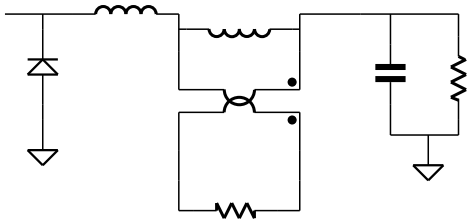
We want to use this transformer as a **current** transformer, so we know **input current**; we can say that:

$$v_{\mathrm{primary}} = \frac{v_{\mathrm{secondary}}}{n}$$

So, the voltage on the secondary winding must be low, and this means that we need small load resistance, ideally zero.

All this stuff is true, in general, for current transformers; in our circuits, with the control loop and the power stage, we have some extra constraints: even if we measure the circuit, we need on R the right output voltage for the controller (so, typically, $V_{\mathrm{secondary,max}} = 1$ V. If the controller reaches 1 V, so the maximum voltage accepted in one cycle, the controller stops the cycle.

We have to find n and R, in order to design the circuit. Let's consider once more our buck converter:

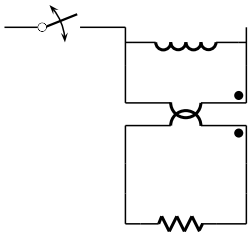


As we know, there are two good sections for current measuring. With current transformers, can we use the section 5 ? Well, it is not good: if we have a DC component, the current through R will generate a voltage with a DC component; the voltage across R'_{S} so is:

$$v_{R'_{\mathrm{S}}} = i_{\mathrm{secondary}} R'_{\mathrm{S}}$$

in the current on the secondary winding there is also the DC component, which will flow to the resistor, generate a DC voltage drop, which will go back, so the primary current starts to ramp up and the transformer saturates: section 5 is not ok.

What about section number 2? Well:



If we put the transformer in series to the switch, does it work? Well, the i_{peak} current is something like what shown in previous graph. i_{SW} has a DC component, so it will saturates. In other words, the pulse goes to the secondary side, and we have a current, on the secondary winding, which is similar (unless the n factor) to the primary one; if we multiply for the load resistance, it has non-zero DC component, so it will charge more and more the inductance at each cycle, and drive into saturation the transformer.

Let's consider a brief numerical example: if we have

$$I_{\text{peak}} = 3 \text{ A}$$

considering $n = 10$ (so an $1 : 10$ transformer), in the secondary winding we have something like:

$$\frac{I_{\text{peak}}}{n} = \frac{3 \text{ A}}{10} = 0.3 \text{ A}$$

In order to satisfy the condition for the maximum voltage of the microcontroller, we have to put a resistance which gives something similar to 1 volt with the maximum current on the secondary winding; this means, using the standard values:

$$R'_{\text{S}} = \frac{1 \text{ V}}{0.3 \text{ A}} \sim 2.7 \ \Omega$$

respect to the resistive solution, which considers a higher current, we have a resistance which is 10 times higher: if we put just a resistance, it will have 3 A on it, so it will be greater of 10 times; what about P_{diss} ? Well:

$$P'_{\text{diss}} = I'^2_{\text{RMS}} R'_{\text{S}}$$

but now we have to evaluate the dissipated power on the **secondary** winding, so we have to use, as current, the RMS current on the secondary winding. We have that, given I'_{RMS} the current on the secondary winding on the transformer (so, in a circuit which measures current with a transformer), and I_{RMS} the current on the measuring resistance (in a circuit which uses resistors to measure current):

$$I'_{\mathrm{RMS}} = \frac{1}{10} I_{\mathrm{RMS}}$$

so, respect to the P_{diss} in a circuit in which we measure the current simply with a resistor:

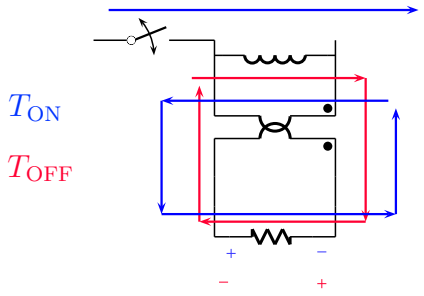
$$P'_{\mathrm{diss}} = R'_{\mathrm{S}} I'^2_{\mathrm{RMS}} = 10 \times R_{\mathrm{S}} \times \frac{1}{100} I^2_{\mathrm{RMS}} =$$

$$= \frac{1}{10} P_{\mathrm{diss}}$$

So, if we measure current from the same section (2) of the same circuit with a transformer instead that with a resistor, we decrease the power dissipation of ten times. This means that:

- we increase the efficiency η of our converter;
- we have smaller components: the value of the resistance is greater respect to the other case, but the dissipated power is smaller, so, generally, components will be smaller; this, means less ESL, so wider band!

We still have a problem: this circuit does not work! In fact, we have something like this:



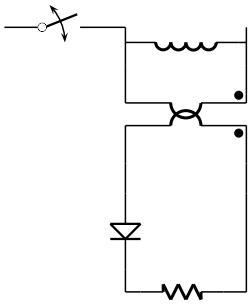
On the load resistor we have something similar to 1 volt voltage drop, during T_{ON}: across the magnetizing inductance, so, we will have something like 0.1 V, and will have some magnetizing current through it. After T_{ON}, we have a time T_{OFF}, when the switch is **open**: it happens that the current of the magnetizing inductance can not flow through the switch, because it is open, so it will go into the transformer, circulate on the secondary winding, and generate a voltage drop on the load resistance, with **opposite sign** (because current in the magnetizing inductance go from left to right, due to the usual conventions; in order to keep the i_{m} be continue, it **must** go with its former direction, so it will generate, in the secondary winding of the transformer, a

voltage drop opposite respect to the T_{ON} one). The voltage across the R'_{S} resistance will be something similar to:

$$v_{\mathrm{S}} = \frac{i_{\mathrm{m}}}{n} R'_{\mathrm{S}}$$

Our goal was the one to reduce errors, so to reduce i_{m}, so it is quite low, and the voltage drop across the R'_{S} resistance, of opposite sign, is quite low: a few percent of the T_{ON} one: instead of the 3 A of our example, something similar to 0.03 A, and so, instead of 1 V voltage drop, a few percent of it: something similar to 0.01 V (just to put some numbers)! This voltage discharges the inductance, but it is too small, so the discharge time is something like 100 times the charge time (the reciprocal of the *few percent*). This means that the magnetizing inductor can only be charged, not discharged, and it will go eventually in saturation.

How may we discharge this magnetizing inductor, with some circuital modifications? Well, we need something which allows current to flow in the right direction, not in the opposite one! This is, simply, a **diode**:



We have that, during T_{ON}, the diode behaves as a short circuit, and we have something like:

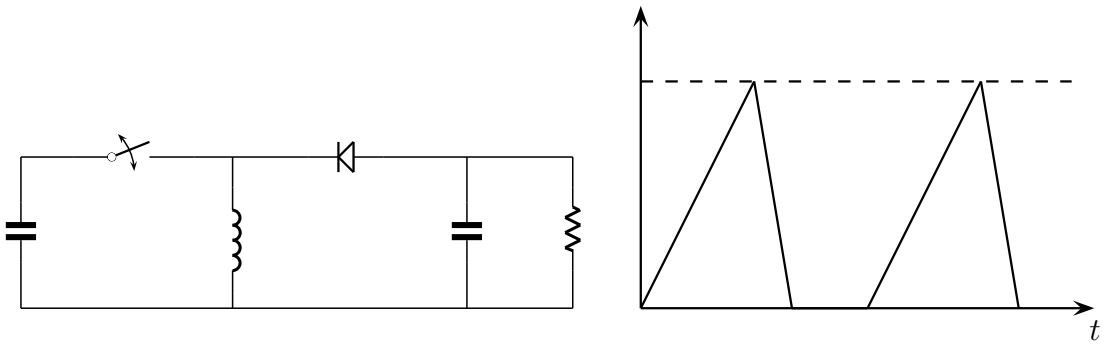
$$T_{\mathrm{ON}} : \frac{i}{n} R'_{\mathrm{S}}$$

Diode actually has a voltage drop, but what does it mean? We are driving this circuit with current, so voltage does not interest us so much!

What about T_{OFF} ? Well, the diode doesn't allows current to go the wrong side, but this current is the current of an inductance: a state variable! This means that this inductance gets mad and its voltage increases, as much as possible to find a path for the current. When voltage increases, it charges all parasitic capacitances, so risks to damage the diode, but the energy storage in the magnetizing inductance is so tiny that this risk does not exist.

Buck-boost current mode

Up to now we talked almost ever about buck converter; let's introduce something about the other important converter we have: the **buck-boost**. We know that:



Still the same story: in buck-boost, we have that current increases, reaches a peak, and so on. In voltage mode we controlled the T_{ON} time; in current mode we want to control the system by setting the i_{peak}, instead of using a PWM modulator.

We used, for the first buck-boost analysis, the energy transfer method:

$$\frac{V_0^2}{R} = \frac{1}{2} f_{\text{SW}} L I_{\text{peak}}^2$$

(we have talked about this expression before)

If we invert this expression, we have:

$$\frac{V_0}{I_{\text{peak}}} = \sqrt{\frac{RLf_{\text{SW}}}{2}}$$

But we don't work directly with current: we want to work with voltages! So:

$$I_{\text{peak}} = \frac{V_{\text{control}}}{R_{\text{S}}}$$

so:

$$\frac{V_0}{V_{\text{control}}} R_{\text{S}} = \sqrt{\frac{RLf_{\text{SW}}}{2}}$$

so:

$$\frac{V_0}{V_{\text{control}}} = \frac{1}{R_{\text{S}}}\sqrt{\frac{RLf_{\text{SW}}}{2}}$$

An observation: in this expression, we are missing the input voltage, V_{IN}! This means that audio susceptibility is ideally 0! This is good, but we still have a problem: in both gain and pole frequency we still have dependence on R, so we have the same situation of buck-boost voltage mode.

Chapter 3

Isolated converters

Now we are going to introduce the isolated, or **derived**, converters. The name **derived** comes from the idea we use: we take a buck, boost (few times) or buck-boost converter, and add a transformer, then see what we can find. We have some advantages and some disadvantages.

Let's start with the advantages.

- We obtain **isolation**: if we touch our PC, for example, we don't get shocked, thanks to the isolation introduced by the transformer. This is not enough: we have to isolate both power stage and control parts.
- We can have multiple output (using more windings of the transformer).
- We have no output voltage limitations, in two senses:
  - we can invert the polarity (so obtain a buck-derived converter with negative output), because what we obtain, respect to the ground of the input stage, is just a floating source;
  - we can have (for example) a buck converter with **higher** output voltage respect to input voltage: no magnitude limitations.
- We have one more extra degree of freedom: the turn ratio (N_S/N_P): this means that (we will understand this statement later) we can choose a convenient duty cycle D (not too short, in order to reduce pulses and so losses);
- We can **move** stresses in the most convenient place of the circuit, or **distribute** them (also this statement will be explained better later).

Now, let's show the disadvantages.

- There is a transformer: the circuit is bigger, more expensive.
- The circuit is more complicated to build and to design.
- We may have some issues about **cross regulation**: cross regulation means to keep all the outputs at the right voltage: if we change the load of one output, we want that all the output stay to the right voltage. If we change load, it may happen that some output voltages of converter V_0 become unstable or change.

Buck converter has a lot of *sons*; the most used are:

- forward converter;
- 2-transistors forward converter;
- push-pull converter;
- half-bridge converter;
- full-bridge converter.

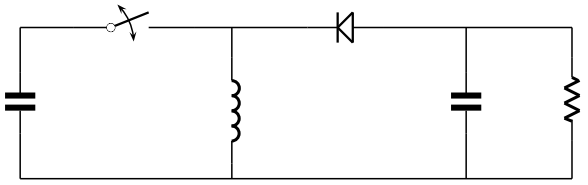
These converters may be useful for high power conversion: they are sons of a buck, so they can be controlled in CCM, and are less stressed.

Boost converter has just one famous derived: the **current fed** converter, which is used few times. About buck-boost, there are two well-known converters: the **flyback** converter, and the **2-transistors flyback** converter.

Flyback is basically the only descendent of the buck-boost, and it is the most used converter in the world: it is quite easy to design, inexpensive, even if it is a son of a boost: if we want to control it (and we want to), we have to use it in DCM, so we are limited to low-power uses.

3.1 Flyback converter

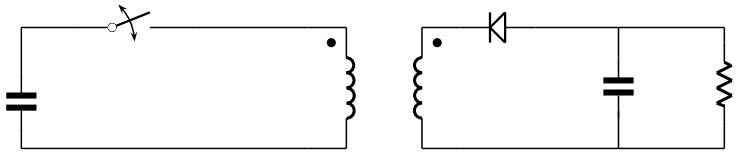
Let's start from the father of our converter: the buck-boost converter



How it works? Well:

- first, we close the switch, and store energy into the inductor;
- then, we open the switch and deliver the stored energy to the output.

Which energy are we storing? Well, at the input we have electric energy (associated to voltages and currents), and we convert it into magnetic energy (magnetic flux) with a transducer: the inductor. Then, we turn it back into electric energy, and deliver in this form to the output. What we can do is something like this:



We can use two windings instead of a single inductor, remembering that buck-boost is an indirect converter: the primary winding will be used just for charging our converter, the secondary just for discharging it.

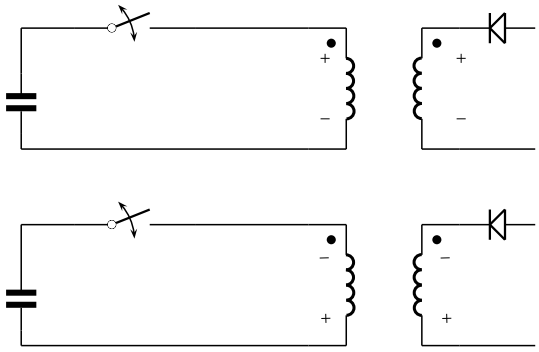
A remark: this is **not** a transformer: those are two **coupled inductors**; the equivalent schematic is something like this:

There is a fundamental difference between a transformer and two coupled inductors: in a transformer we wanted a very high magnetizing inductance, no matter its value; now, we want a **finite** and **controlled** L_p value (where L_p is again the magnetizing inductance, and "p" means **primary**, because we usually put it into the primary winding, even if it is not mandatory). Magnetizing inductance, in fact, is a model which represents the fact that this device can store energy!

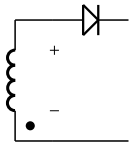
Now, our goal is to **store** energy, so we **need** a particular inductance.

Let's analyze this converter:

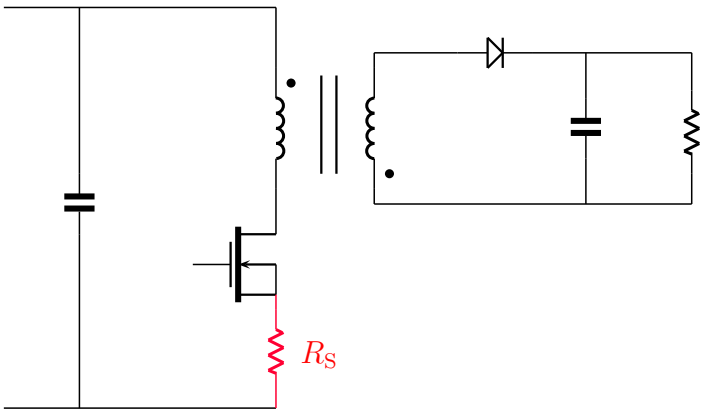
- when we close the switch, V_P is positive; if we have a positive voltage on a dot, we know that all positive voltages will be on all the dots of the transformer; at this state, diode is in cut-off;
- if we open the switch, diode is conducting, so voltages are reversed.



Now, just for cosmetics, we can change this schematic into this:



Now, we have something slightly different respect to what we had: we don't have the diode connected to the inductance, so we can say that switch and primary winding are in **series**, and this means that we can **swap** them, obtaining something like this:

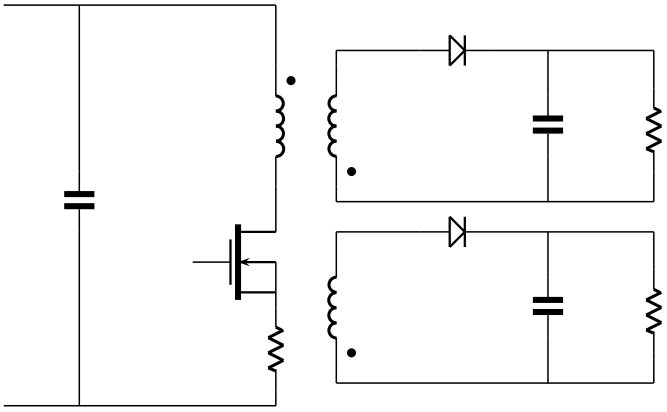


Now we have that the transistor is referred to the **floor**, so it is a **low-side** transistor: this is much more easier to drive!

If we want to use current-mode control, we must sense the inductor current; we want to sense it during T_{ON}, so we **have** to use the primary winding; we can use a resistor referred to ground! This is good, because the voltage we have over here, $i_L R_S$, is referred to ground, so we don't have to sense high voltages.

This converter is inexpensive: we have one magnetic core (with some windings), it is isolated, and we can use low-side switches: for these reasons, this is the best topology for low power levels.

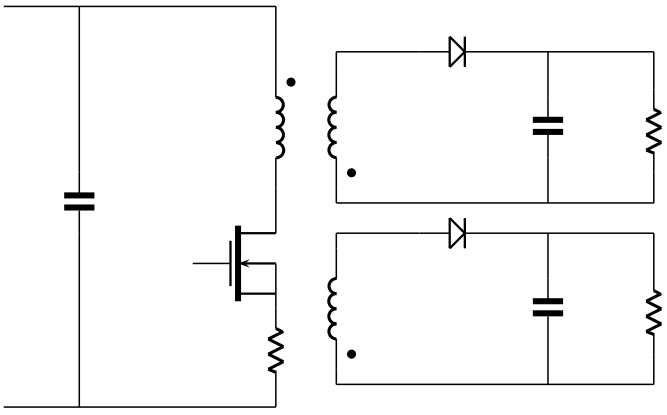
If we need two output voltages, we still have our coupled inductors, but we can just add another secondary winding:



Just a remark: if we use current mode, we may have the sense resistor, so we have the switch not referred to ground; the good thing is that the maximum voltage across the R_S resistor is of 1 volt, so it doesn't matter.

3.1.1 Flyback analysis

We are going to analyze our converter, in a similar way to the buck-boost one, considering the extra degree of freedom we have. We consider the two-outputs topology, in order to show a general case.



Our goal is to determine stresses, turn ratios, value of the magnetizing inductance. We **can** use current mode, and so put or not R_S: in buck-boost

derived we don't have many advantages like in buck, but we have circuit protection against short circuits, and small audio susceptibility.

As hypothesis, we will consider cyclostationary condition, small output ripple, high time constant, but also **losses**: now we are going to consider the voltage drops across diode and switch.

Turn ratio

Let's start from the turn ratio: the two secondary windings are taking energy from the magnetic core; the important point is to remember that:

$$\frac{\partial \phi}{\partial t} = \frac{\partial \left[\mathbf{b} \cdot \mathbf{s} \right]}{\partial t}$$

Each one of the windings senses the same variation of the magnetic inductance vector $\mathbf{b}$; from Physics we know that:

$$\frac{\partial \phi}{\partial t} = -V$$

where V is a **voltage**; how much are the voltages on the windings? Well, this depends on the number of turns we have:

$$\frac{N_{\mathrm{S1}}}{N_{\mathrm{S2}}} = \frac{V_{\mathrm{S1}}}{V_{\mathrm{S2}}} = \frac{V_{01} + V_{\mathrm{D2}}}{V_{02} + V_{\mathrm{D2}}}$$

The voltage on one of the secondary windings equals the sum of the output voltage and the voltage drop on the diode.

In order to avoid saturation status, we **need** that:

$$\overline{V}_{\mathrm{winding}} = 0$$

If we are not in control mode, the saturated inductor becomes a piece of wire, so we have unlimited current (because we don't have the short-circuit control protection), and we destroy the MOS transistor. We know that, given the energy of the primary inductance (stored into magnetic flux):

$$P_0 = E_{L_{\mathrm{p}}} f_{\mathrm{SW}}$$

Those are the basic equations we need to design the coupled inductors. There is another condition, given by common sense: the **stress moving**: the turn ratio is an extra parameter, and it permits to change D, the duty cycle; this permits to move (as already said) the stresses in the various parts of the circuit. Be careful: this **does not mean** that we can **reduce** stresses, we can just **move** them, but this means that we can have relaxed components!

A common sense choice for moving stresses may be this one: given D the duty cycle of the charging phase, and D_2 the duty cycle of the discharging phase (because we are not in CCM, so there is also an idle time),

$$D + D_2 < 1$$

we **have to** stay in DCM, so the sum of the two duty cycles must be less than one.

If there are no other constraints, a reasonable choice may be to choose:

$$D_{\max} = D_{2,\max}$$

Same times to charge and discharge the circuit. How much less than 1? Well, we have to stay close to 1 (in order to use the converter for a good time), but not too close (due to tolerances): 0.3 is too low (we are using the converter just for 30% of the time), but 0.99 is too much; good choice are 0.9, 0.85, 0.8.

Output power

How much is the output power? Well, we have two output voltages, so two powers (let's remark that these flyback converters work well with 2 or 3 secondary windings, but with 4 the cross regulation becomes very worse); we have that:

$$P_0 = \sum_i V_{0\mathrm{i}} I_{0\mathrm{i,max}} \sim (20 \div 70) \ \mathrm{W}$$

this gives us an idea of which is the output power: the total power delivered to the output.

Let's go back: the total power to the secondary windings will be something similar:

$$P_{\mathrm{secondary}} = \sum_i \left(V_{0\mathrm{i}} + V_{\mathrm{Di}}\right) I_{0\mathrm{i,max}}$$

given the output current, we just have to multiply it for the sum of output voltage and voltage drop on the diode.

Going back, we want to find the power into the primary winding: it is just the power which enters in the primary winding! In order to evaluate it, there is a *magic factor* which considers dissipations and all that stuff:

$$P_{\mathrm{primary}} = \frac{P_{\mathrm{secondary}}}{\eta_{\mathrm{magnetic}}}$$

where η_{magnetic} is the **magnetic efficiency**; we have that:

$$\eta_{\text{magnetic}} = 0.85 \div 0.9$$

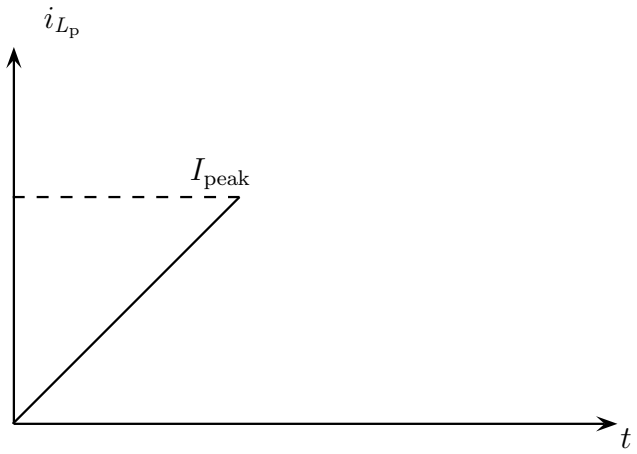
Now, from primary power, we can evaluate primary energy:

$$E_{\text{primary}} = \frac{P_{\text{primary}}}{f_{\text{SW}}}$$

f_{SW} is another degree of freedom: we can choose it! But... We have to stay into low frequency ranges: $100 \div 200$ kHz! Isolated topologies have transformers, so they must work with lower frequencies.

Given the energy on the primary winding, we can use, with L_{p} inductance, the standard equation:

$$E_{\text{primary}} = \frac{1}{2} L_{\text{p}} I_{\text{peak}}^2$$



when we open the switch, the current on the primary inductance goes to zero; we obtain that the D we use is, in order to stay in DCM:

$$D_{\max} T_{\text{SW}}$$

the slope of this curve will be:

$$\frac{\mathrm{d}i_{L_{\text{p}}}}{\mathrm{d}t} = \frac{V_{L_{\text{p}}}}{L_{\text{p}}} = \frac{V_{\text{IN,min}} - V_{\text{SW}} - V_{R_{\text{S}}}}{L_{\text{p}}}$$

where the R_{S} term is there **just in current mode**.

Why minimum values? Well, if we want to obtain a certain input current, we have to use, as critical voltage, the one which gives more problems: the minimum input current corresponds to the minimum input voltage; we have

so this equation. As V_{R_S} we can use 1 V (this is an approximation: this voltage is variable, but we may just take the worst value, so the maximum one). About V_{SW}, we know that the closed switch behaves as a resistance, so we can use the maximum; we ask V_{SW} to be a few percent of the input voltage, and choose the switch with this constrain. Now, from this equation, we can find our L_p:

$$I_{peak} = \frac{V_{IN,min} - V_{SW} - V_{R_S}}{L_p} D_{max} T_{SW}$$

we can substitute it into our $E_{primary}$ expression:

$$E_{primary} = \frac{1}{2} L_p \left(\frac{V_{IN,min} - V_{SW} - V_{R_S}}{L_p} \right)^2 D_{max}^2 T_{SW}^2$$

L_p is the unknown: we can just reverse this equation, and obtain:

$$L_p = \frac{1}{2} \frac{I_{peak}^2}{E_{primary}} \left(V_{IN,min} - V_{SW} - V_{R_S} \right)^2 D_{max}^2 T_{SW}^2$$

by arranging:

$$L_p = \frac{\left(V_{IN,min} - V_{SW} - V_{R_S} \right)^2}{2 \frac{P_{secondary}}{\eta_{magnetic}} f_{SW}} D_{max}^2$$

This is the maximum value of L_p: we have to take a value which is less or equal to this one.

Now: we want, in order to avoid saturation, that the average voltage on each winding is zero; in order to do it, which is the voltage on the primary winding? Well:

- during T_1:

  $$V_p = V_{IN} - V_{SW} - V_{R_S}$$

  actually, we can just say that

  $$V_p \sim V_{IN}$$

- during T_2, the switch is open, diodes are conducting, and we have to find the voltage over the secondary, then bring it back to the primary! So:

  $$V_p = - \left(V_{01} + V_{D1} \right) \frac{N_p}{N_{S1}}$$

- during T_{idle}, all currents and voltages are zero.

Now, we know, for all times, the voltages; we have to evaluate the average, and set it equal to zero:

$$(V_{\text{IN}} - V_{\text{SW}} - V_{R_{\text{S}}})\, D - (V_{01} + V_{\text{D1}})\, \frac{N_{\text{p}}}{N_{\text{S1}}} D_2 = 0$$

we want to find the turn ratio:

$$\frac{N_{\text{p}}}{N_{\text{S1}}} = \frac{(V_{\text{IN}} - V_{\text{SW}} - V_{R_{\text{S}}})\, D}{(V_{01} + V_{\text{D1}})\, D_2}$$

this is the last equation we need to determine the parameters to design our magnetic component.

Now, we can assume to have

$$D_{\max} \sim D_{2,\max} \sim 0.4 \div 0.5$$

this is just an initial choice: we have to take account of the stresses, and we are going to evaluate them.

Voltage stresses

The most stressed components are the diode and the switch; under the voltage stresses point of view, the worst states are the **off** ones: when diode or switches are not conducting.

What about the diode, when it is off? Well, from one side we have the output voltage; to the other side, the secondary voltage, which equals:

$$V_{\text{D}} = V_0 + V_{\text{IN}} \frac{N_{\text{S}}}{N_{\text{p}}}$$

we are considering just one diode, so don't specify the subscript; this is true for all elements. We forgot the switch and sense-resistance voltage drops, but this is ok: this is an upper bound case!

In order to determine the max stress, we have to take the maximum V_{IN}.

About V_{SW}, the maximum voltage drop across it is when it is open; we have to start from the secondary side, and find that:

$$V_{\text{SW}} = V_{\text{IN,max}} + (V_0 + V_{\text{D}})\, \frac{N_{\text{p}}}{N_{\text{S}}} + (0.2 \div 0.3)\, V_{\text{IN}}$$

the last term derives from the **leakage inductance**: this comes from the fact that our magnetic component is not ideal! We have a leakage inductance

in series to the primary winding, and its magnetic flux lines are not concatenated to the secondary winding: this is leakage because, even if it doesn't dissipate any power, it does not bring power contributes to the secondary windings.

Leakage inductance has an energy, so when we open the switch it has no way to discharge, and we have an overvoltage which increases the voltage stress on the switch.

A remark: V_{SW} and V_{D} stresses depend on the turn ratio: if we change the turn ratio, we change the stresses on the components; we have to care about the fact that we have to change also D and D_2!

This is what we said: with the transformer, we have an extra degree of freedom, and we can **move** the various stresses from one side to another of the circuit.

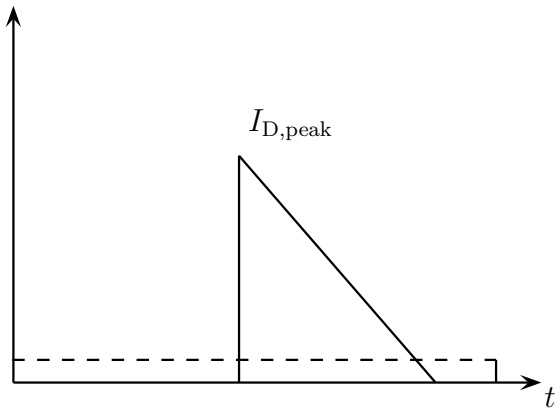
Current stresses

In order to determine the current stresses, we have to evaluate $\overline{i}_{\mathrm{D}}$, and $I_{\mathrm{D,peak}}$; same thing for the switch: $\overline{i}_{\mathrm{SW}}$, and $I_{\mathrm{SW,peak}}$. How to do it?

For $\overline{i}_{\mathrm{D}}$ we can use KCL (average is a linear operation!), so see that:

$$\overline{i}_{\mathrm{D}} = I_0$$

a **bad** idea is to find $I_{\mathrm{D,peak}}$ from the winding current: with two windings it is very difficult to do; what we may use is a smarter idea:



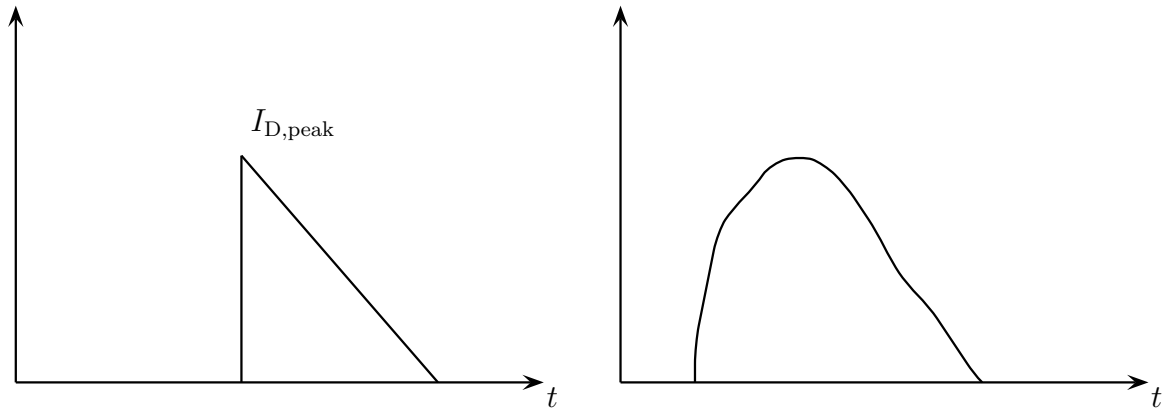
We know the average voltage, so we can reverse the average operation; we know that:

$$\overline{i} = I_{\mathrm{peak}} \frac{D_2}{2}$$

so

$$I_{\mathrm{D,peak}} = \frac{2I_0}{D_2}$$

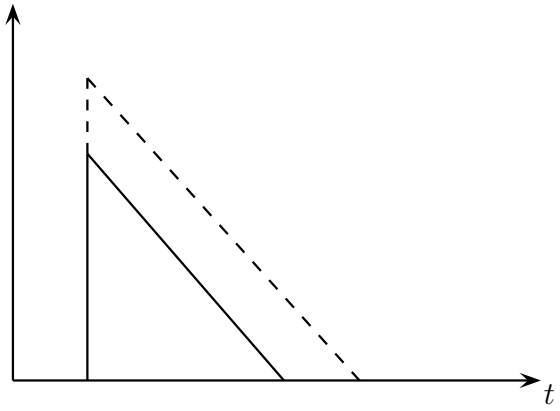
A remark: D_2 is basically **the same** for all secondary windings; this means that they stop at the same time.



these are the waveforms we ideally have. Actually, as we can see in the second graph, they are slightly more complicated: due to leakage inductances on the secondary windings, we have some complications.

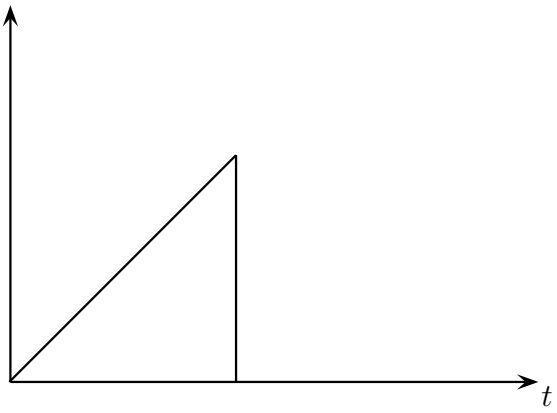
Now, in order to evaluate the worst stresses, we need the **maximum** output current: we know that D depends on V_{IN} and P_0: D increases as V_{IN} decreases, and P_0 increases.

What about D_2? Well, on the output, we have that, if we need more power, we have to increase this ares:



in order to do it, we have to make it higher and longer, so we have to take the maximum D_2: it is not independent to I_0 so we have it.

What about the switch? Well, the current on the switch is something like this:



$$\bar{i}_{\mathrm{SW}} = \frac{I_{\mathrm{SW,peak}} D_{\max}}{2}$$

where, since we know the slope:

$$I_{\mathrm{SW,peak}} = \frac{V_{\mathrm{IN}} - V_{\mathrm{SW}} - V_{R_{\mathrm{S}}}}{L_{\mathrm{p}}} D T_{\mathrm{SW}}$$

Now, it seems that we need both maximum D and V_{IN}; this is not true, because the two quantities are correlated: if D increases, we want a constant peak current, so slope decreases, and also V_{IN}!

Let's consider the fact that we don't know $D_{\min}$: a good idea may be the one to use $D_{\max}$ as parameter, so:

$$I_{\mathrm{SW,peak}} = \frac{V_{\mathrm{IN,min}} - V_{\mathrm{SW}} - V_{R_{\mathrm{S}}}}{L_{\mathrm{p}} f_{\mathrm{SW}}} D_{\max}$$

May we change $D_{\max}$ and D_2? Well, of course! We just **assumed** the values! But... If we want to reduce the peak current, we can change $D_{\max}$, D_2, and I_{peak}; our problem is that, if we increase D_2, we have to decrease $D_{\max}$, in order to maintain the DCM

$$D_2 + D_{\max} < 1$$

but, if we decrease $D_{\max}$, we increase I_{peak}, because of the D^2 dependence of L_{p}. Let's see some equations:

$$I_{\mathrm{SW,peak}} = \frac{V_{\mathrm{IN,min}} - V_{\mathrm{SW}} - V_{R_{\mathrm{S}}}}{L_{\mathrm{p}} f_{\mathrm{SW}}} D_{\max}$$

but

$$L_{\mathrm{p}} = \eta_{\mathrm{magnetic}} \frac{\left(V_{\mathrm{IN,min}} - V_{\mathrm{SW}} - V_{R_{\mathrm{S}}}\right)^2}{2P_{\mathrm{secondary}} f_{\mathrm{SW}}} D_{\mathrm{max}}^2$$

so, combining the two:

$$I_{\mathrm{SW,peak}} = \frac{\left(V_{\mathrm{IN,min}} - V_{\mathrm{SW}} - V_{R_{\mathrm{S}}}\right) D_{\mathrm{max}} 2 f_{\mathrm{SW}} P_{\mathrm{secondary}}}{\eta_{\mathrm{magnetic}} \left(V_{\mathrm{IN,min}} - V_{\mathrm{SW}} - V_{R_{\mathrm{S}}}\right)^2 D_{\mathrm{max}}^2}$$

so

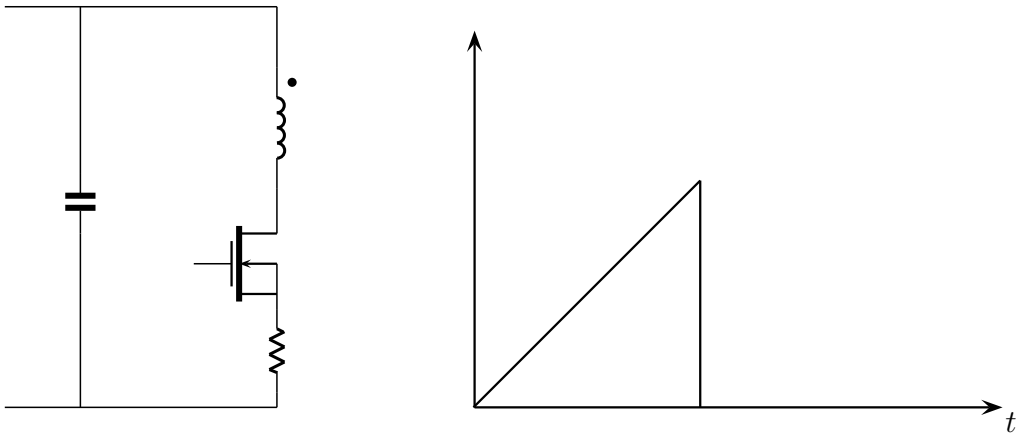
$$I_{\mathrm{SW,peak}} = \frac{2P_{\mathrm{secondary}}}{\eta_{\mathrm{magnetic}} \left(V_{\mathrm{IN,min}} - V_{\mathrm{SW}} - V_{R_{\mathrm{S}}}\right) D_{\mathrm{max}}}$$

If we increase D_2, we have to decrease D_{max}, but so current goes up.

There is another issue: if we increase D_2, we have to decrease D_{max}, so $I_{\mathrm{D,peak}}$ decreases, $I_{\mathrm{SW,peak}}$ increases, but, if we consider also the turn ratios, they change, and move the voltage stresses! Switch voltage stress decreases, but diode voltage stress increases!

Primary winding stresses

Which are the stresses on the primary winding? Well, we have to evaluate RMS and peak current for the primary inductance, L_{p}:



$$I_{L_{\mathrm{p}},\mathrm{peak}} = I_{\mathrm{SW,peak}}$$

What about RMS? Well, we may use the simplified equation, and find that:

$$I_{\mathrm{RMS}} = I_{\mathrm{peak}} \sqrt{\frac{D_{\max}}{3}}$$

we use the maximum duty cycle $D_{\max}$ in order to consider the maximum RMS current.

What about the R_{S} sense resistance for current mode? Well:

$$R_{\mathrm{S}} = \frac{1\ \mathrm{V}}{I_{\mathrm{peak,max}}}$$

and

$$P_{\mathrm{diss}} = I_{\mathrm{RMS}}^2 R_{\mathrm{S}}$$

Capacitors stresses

What about the capacitor stresses? Well, we have two capacitors: input and output (actually, more than one output capacitor: one for output!).

For input capacitor, there are (due to its lucky position) two important values: voltage, and RMS current (ESR is not important because this is a low-stressed capacitor, and because ESR controls the ripple). In order to evaluate RMS value, we can use the *quasi*-KCL:

$$I_{C_{\mathrm{in}},\mathrm{RMS}} = \sqrt{I_{\mathrm{RMS}}^2 - I_{\mathrm{DC}}^2} = \sqrt{I_{\mathrm{peak}}^2 \frac{D_{\max}}{3} - \left(I_{\mathrm{peak}} \frac{D_{\max}}{2} \right)^2} =$$

this, using the Nutella theorem; arranging:

$$= I_{\mathrm{peak}} \sqrt{\frac{D_{\max}}{3} - \frac{D_{\max}^2}{4}}$$

What about output capacitors? Well, we have to evaluate three parameters:

- working voltage (which equals the **output voltage**);
- I_{RMS}: same story as before! By simple math, we can easily proof that the formula equals (with some changes) the previous one:

$$I_{C_0,\mathrm{RMS}} = I_{\mathrm{peak}} \sqrt{\frac{D_2}{3} - \frac{D_2^2}{4}}$$

- if we have a ceramic capacitor, we have to specify the capacitance value (by taking the capacitance equation, integrating it, and obtaining the amount of charge over C; if we have an electrolytic capacitor, we have to find the R_{ESR}, which controls the output voltage ripple, and use it in order to choose the capacitor model.

3.1.2 Power losses in switches

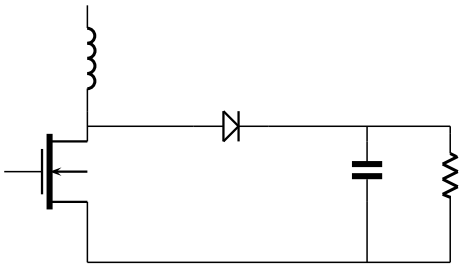
In switches, we have two kinds of losses:

- conduction losses (which can be evaluated simply by calculating $r_{\text{ds,on}}$ times $I^2_{\text{SW,RMS}}$);
- switching losses: losses which happen each time we open or close the switch.

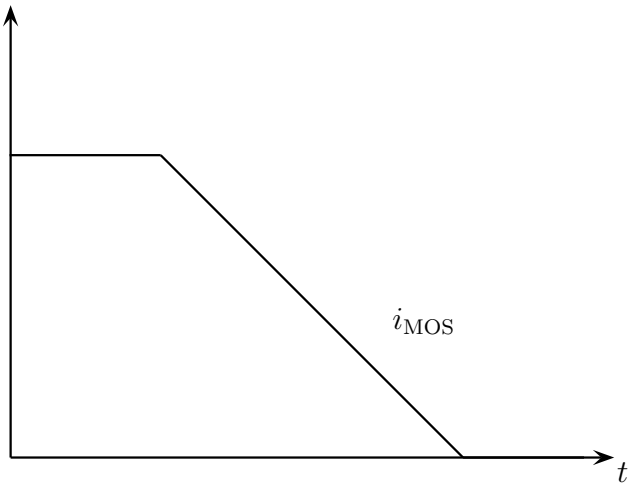
The most important losses in switches are the last ones.

Why do we have those losses? Well, let's consider an ideal switch: when it is closed, it is similar to a piece of wire; when it is open, it is similar to an open circuit. What we didn't consider is what happens **in between**! We open and close the switch in a non-zero time! This means that, for a time, we have both current and voltage which are non zero! This, for both opening and closing situations!

All our switches have an inductive load:

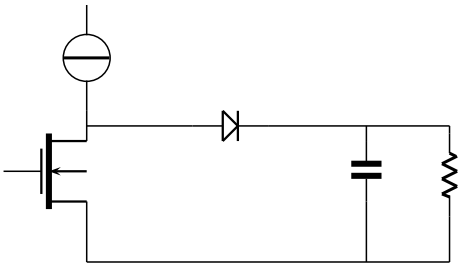


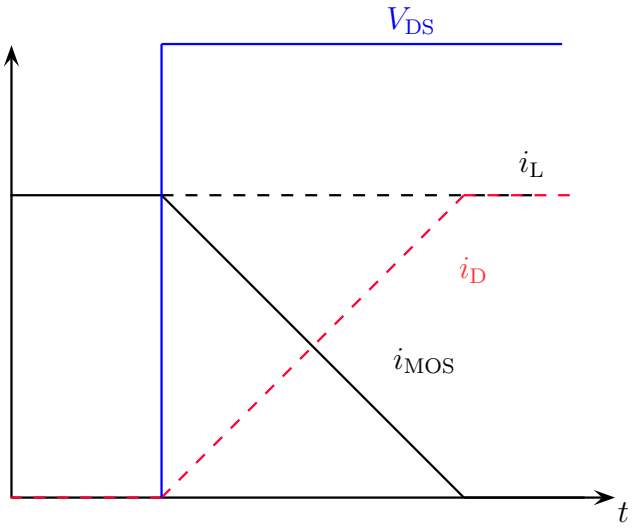
This is an example, with a **boost** converter. What happens when the switch open and closes? Well, we can use this model for this switch:



What we assume is that current goes down linearly; and t_{off} is the **turn-off time**. Current is constant, because $t_{\text{off}} \ll T_{\text{SW}}$, so we can see it as a constant value. In MOS, $t_{\text{off}} \sim 0.1\ \mu$s.

For a short period of time, we can say that an inductor behaves as a constant current source; just for t_{off}, so, we can analyze this circuit:





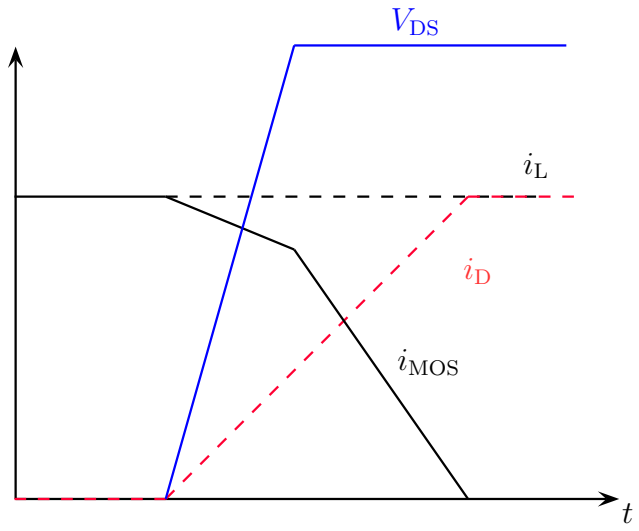
Let's suppose that current is for example 3 A: the switch doesn't want to stop 3 A instantly, but asks just for less current. i_L is constant, i_{MOS} decreases linearly, and so the extra current (the difference of the inductor and the MOS current) goes into the diode.

Bad news: V_{DS} voltage is 0 before the starting time, because transistor is *closed*; if we increase the current on the diode, we turn it on: in order to

make a diode be conductive, we must accept a voltage drop on it; when we have both current and voltage, we have power dissipation!

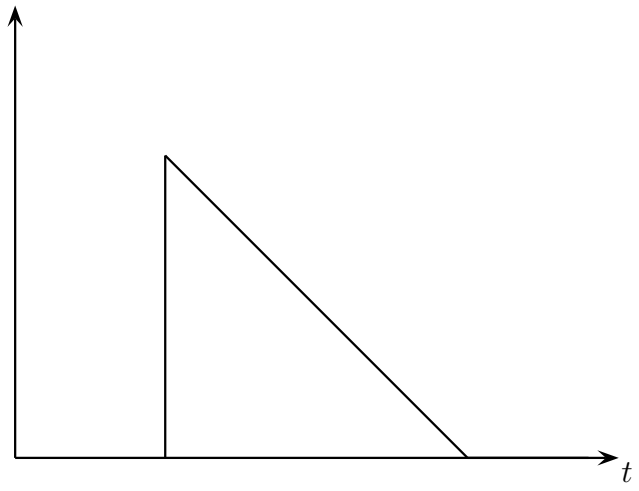
$$V_{\mathrm{DS}} = V_{\mathrm{D}} + V_0$$

Actually, we have something like this:



There is a time for charging all capacitances, and then to make voltage increase; so, once we charged the capacitances, the current slope decreases.

The ideal instantaneous power is something like this:



voltage stays constant, current goes down, and so power goes down with the same behaviour of the current: in this model, linearly.

We care especially about average power: the energy lost in each opening action is just the area of the previous curve. We have so to calculate the area of a triangle:

$$E_{\text{lost}} = \frac{V_{\text{SW}} I_{\text{SW}} t_{\text{off}}}{2}$$

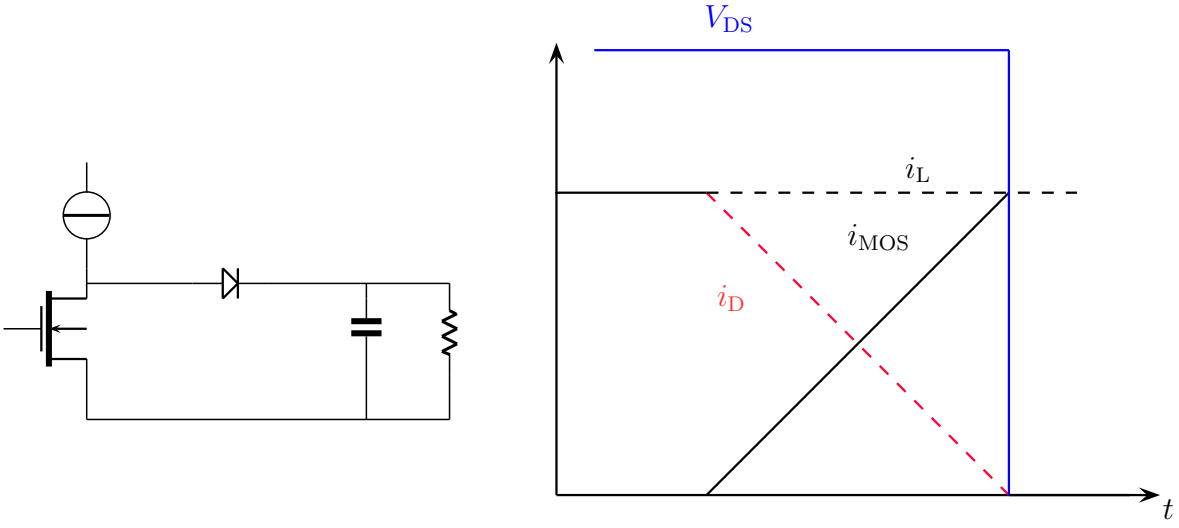
Where V_{SW} is the voltage **after** that the switch opens, I_{SW} the current we have on the switch **before** it opens. We can find the power simply by multiplying it for f_{SW}:

$$P_{\text{lost}} = \frac{V_{\text{SW}} I_{\text{SW}} t_{\text{off}}}{2} f_{\text{SW}}$$

V_{SW} is known; I_{SW} may be determined from the power level of the converter; t_{off} can be decided by choosing the MOS; f_{SW} is a degree of freedom of our design, but we can't choose it too low: lowest the frequency, biggest the devices!

Turn-on losses are exactly the same: we just have to read from right to left the last graph, in order to obtain the same thing. We still have the constant current generator instead of the inductor, the closing switch, the diode, but now the switch asks for more current, not for less current! DCM shows us an advantage, now we have that $I_{\text{min}} = 0$, so we have **no turn-on losses** in DCM.

What about MOS voltage? Here, diode conducts until switch is closed, so we have voltage across it until we have current on the diode; we still have a triangular waveform:



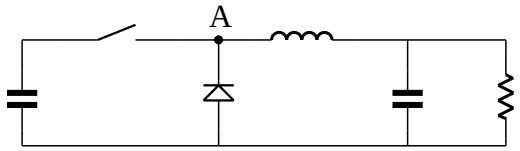
we have:

$$P_{\text{loss}} = \frac{V_{\text{SW}} I_{\text{SW}} t_{\text{on,sw}}}{2}$$

where V_{SW} is the voltage across the switch before the closing process, and I_{SW} is the current across the switch after the closing process.

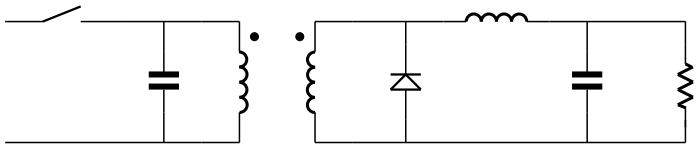
3.2 Forward converter

We are going to introduce a converter which derives from the **buck converter**. A first step so may be to remember how a buck converter is:



We want to add, to this converter, a transformer. A transformer can not handle DC voltage, due to saturation, so we must add it into points with AC components: input or output are bad points!

We may do something like this:



Let's remember that buck is a direct converter; this means that this must be a transformer, not two coupled inductances: with coupled inductances our purpose was to store energy as magnetic field, now just to obtain something similar to a transformer; this means that the magnetizing inductance L_{p} must be the highest we can obtain.

We have magnetics; this means that, for every winding, we have to be sure to have:

$$\overline{v}_{\text{winding}} = 0$$

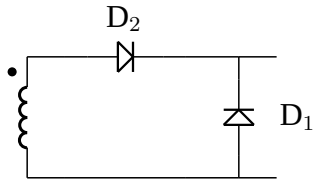
Let's analyze this topology: when we close the switch, we put V_{IN} to the primary winding; this means that we have a positive voltage to the dot. When we open, the diode closes, so we have something similar to zero as voltage on the secondary winding; this reflects into the primary winding:

- $T_{\text{ON}}: \quad V_{\text{p}} = V_{\text{IN}}$
- $T_{\text{OFF}}: \quad V_{\text{p}} = 0$

This behaviour has a DC component (an average) which is different from zero.

How to solve this problem? Our problem is the diode D: it is forcing the connection to ground, during T_{OFF}: we can't go under ground, due to this diode.

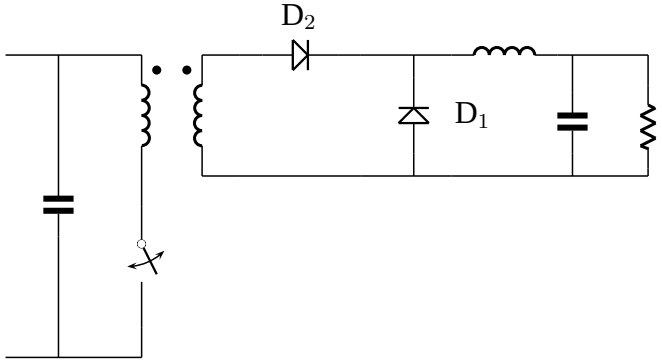
Our solution may be this one:



This diode behaves like this:

- during T_{ON} we apply positive on dots, so D_2 is on, D_1 is off, and we deliver energy to the output;
- during T_{OFF}, the L_{p} makes all polarities change: we have that diode D_2 is off, and D_1 is on; on the node A we have 0 volt, and D_2 impose a reverse voltage, which is a negative voltage; this permits to reduce the flux, without bringing nothing to the output: this diode decouples D_1 and the secondary winding.

Now, let's consider the equivalent circuit for this transformer (we can swap switch and transformer because they are in series):

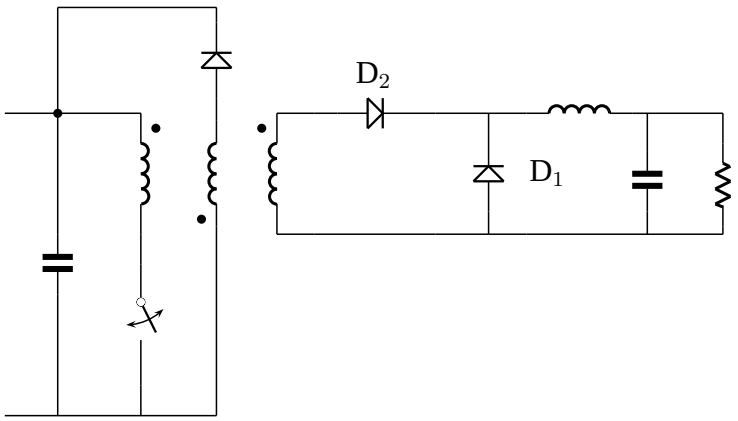


What happens for i_{m}? Well:

- during $T_{\rm ON}$, we have the same result of all times: across $L_{\rm m}$ we have a positive voltage with plus on top, so $i_{\rm m}$ increases and we store in it energy, as magnetic flux;

- during $T_{\rm OFF}$, the switch open, so D_2 opens, D_1 closes, and $i_{\rm m}$ keeps going; $i_{\rm m}$ goes to the transformer, through the non-dot side, but here can not flow: D_2 does not allow current to go through this direction; this means that our switch and D_2 will go in breakdown.

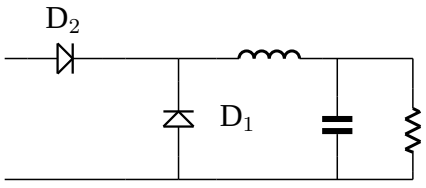
We need to provide some path to $i_{\rm m}$: after storing energy in this inductance, we have to release it, in order to prevent saturation! What we can do in order to solve this problem, to provide this path for the magnetizing inductance current, we have to add another winding, just to remove energy in a controlled way from the magnetic core. The idea can be realized in the following way:



This third winding has some kind of tiny-flyback on it: it is an extra-converter which must just remove the energy from the magnetizing inductance, just to prevent the saturation of the magnetic core. This energy can be recovered, simply by connecting this tiny-flyback to the input.

Now, let's calculate all the stresses and design equations for this converter.

Let's start from $V_0(V_{\rm IN})$: from the secondary winding up, we have a buck converter:



this means that, starting from the secondary voltage V_S, we have:

$$V_0 = DV_S$$

if we want to be more precise, we can release the ideal-diode approximation:

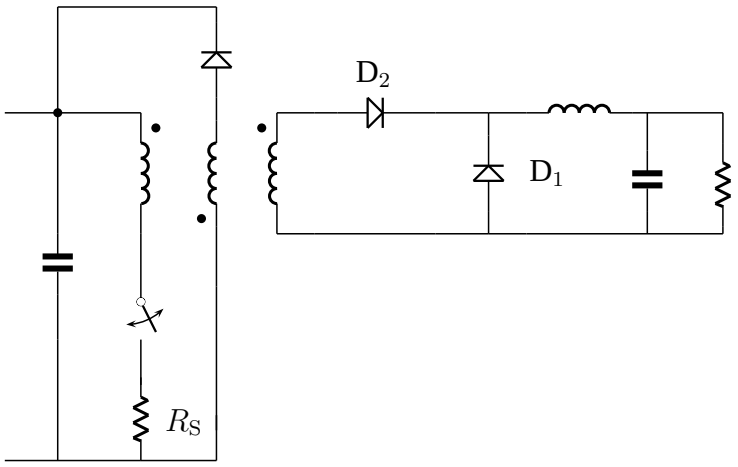
$$V_0 = DV_S - V_D$$

This is true for both T_{ON} and T_{OFF} times: during T_{ON} the voltage drop comes from D_2; during T_{OFF}, from D_1. In order to be very precise, V_D is the average of the diodes voltage drops, but if we assume that $D_1 \sim D_2$, we have the same V_D, so it equals the average. We can write V_S as function of the voltage on the primary winding, so:

$$V_0 = (V_{IN} - V_{SW} - V_{R_S}) \frac{N_S}{N_P} D - V_D$$

The R_S voltage drop as usual is here only if we design for current mode: with voltage mode controllers, we don't have anything which senses the current, so any other voltage drop.

If we remember the various positions from where we can sense current, we can remember that there are two good places for the sense resistance; the best solution is this one:



This is the best solution, because R_S is connected to ground; current mode is very good because now R_S protects the switch from the transformer saturation.

We showed one equation; now, the second equation, is this one:

$$L > \frac{(1 - D_{\min})R_{\max}}{2f_{\mathrm{SW}}}$$

this is the classical buck design equation.

Respect to the buck case, we have an extra degree of freedom: the turn ratio! We can choose the duty cycle and determine $N_{\mathrm{S}}/N_{\mathrm{P}}$. Usually, what we do in the previous equation (not the L one) is to choose $V_{\mathrm{IN,min}}$ and $D_{\max}$, obtaining:

$$V_0 = (V_{\mathrm{IN,min}} - V_{\mathrm{SW}} - V_{R_{\mathrm{S}}}) \frac{N_{\mathrm{S}}}{N_{\mathrm{P}}} D_{\max} - V_{\mathrm{D}}$$

this, because we know that the maximum duty cycle is limited by L_{m}: we have a very short $1-D$, and it means that we can't discharge our transformer, because time is too short.

What about the tertiary winding? Well, as first choice, we may use

$$\frac{N_{\mathrm{T}}}{N_{\mathrm{P}}} = 1$$

usually, this is a good choice, for two reasons: the first one will be explained later; the second one is that, when we wind the primary winding, we have to remember that i_{m} is a very small current; what we can do is to turn the wires together with the primary winding wires, but just in the interstices between two *big* wires:

Now, let's remember our main constraint: in order to prevent magnetics saturation, we must have:

$$\overline{V}_{\mathrm{P}} = 0$$

but we know that:

- during T_{ON}:

$$V_{\mathrm{P}} = V_0$$

- during T_{OFF}:

$$V_{\mathrm{P}} = -V_{\mathrm{IN}} \frac{N_{\mathrm{P}}}{N_{\mathrm{T}}}$$

Given this idea, we may evaluate the average voltage, and put it equal to zero:

$$\overline{V}_{\mathrm{P}} = DV_{\mathrm{IN}} - (1-D)V_{\mathrm{IN}}\frac{N_{\mathrm{P}}}{N_{\mathrm{T}}} = 0$$

so we can reverse this equation and find:

$$D - \frac{N_{\mathrm{P}}}{N_{\mathrm{T}}}(1-D) = 0$$

so

$$\frac{N_{\mathrm{P}}}{N_{\mathrm{T}}} = \frac{D}{1-D}$$

Now: we said that a good initial choice may be to have $N_{\mathrm{P}} = N_{\mathrm{T}}$; in this case, we obtain, from the previous equation, $D = 0.5$.

This equation explains us something: if we increase the magnetic flux for a time, we have to decrease it for the same time, in order to have, at the end of each cycle, zero flux into the magnetic core, and prevent saturation.

If we reverse the previous equation, we can find a relation between D and the primary-to-tertiary turn ratio:

$$D = \frac{\frac{N_{\mathrm{P}}}{N_{\mathrm{T}}}}{1+\frac{N_{\mathrm{P}}}{N_{\mathrm{T}}}}$$

This means that if we choose a different turn ratio, we can increase the duty cycle; for example, if we choose $N_{\mathrm{P}}/N_{\mathrm{T}} = 3$, we have $D_{\max} = 0.75$. This is just a little increase of the duty cycle, but which introduces very bad side effects, on the voltage and current stresses.

Device stresses

For every diode, we need three quantities: I_{peak}, $\overline{i}_{\mathrm{D}}$, V_{reverse}. Let's calculate them for each of the three diodes.

- For D_1, we have that the peak current is the inductor peak value, and we know it:

  $$I_{\mathrm{peak},1} = I_0 + \frac{1}{2}\frac{V_0(1-D)}{Lf_{\mathrm{SW}}}$$

  about the average current, it is just I_0, during a normalized time $1-D$:

$$\overline{i}_{\mathrm{D}_1} = I_0(1-D)$$

about the reverse voltage, we have to see what happens into the primary winding, and brind it to the secondary; when the diode is open, the switch is open, so we have:

$$V_{\mathrm{reverse}} = V_{\mathrm{IN,max}}\frac{N_{\mathrm{S}}}{N_{\mathrm{P}}}$$

- For D_2, we have to evaluate all these quantities. About the peak current, nothing new: just the inductor's one; about average voltage, instead of during the T_{OFF} time, this works just during the T_{ON} time, so we have something like:

$$I_{\mathrm{peak},2} = I_0 + \frac{1}{2}\frac{V_0(1-D)}{Lf_{\mathrm{SW}}}$$

$$\overline{i}_{\mathrm{D}_2} = I_0 D$$

about the reverse voltage, we have something different: this diode has, when it is reversely biased, at the right pin a voltage close to zero, and at the left pin, the secondary voltage. This diode works together with the third winding, so we have to refer the secondary voltage to the tertiary voltage, which is V_{IN}:

$$V_{\mathrm{reverse}} = V_{\mathrm{IN}}\frac{N_{\mathrm{S}}}{N_{\mathrm{T}}} = V_{\mathrm{IN}}\frac{N_{\mathrm{S}}}{N_{\mathrm{P}}}\frac{N_{\mathrm{P}}}{N_{\mathrm{T}}}$$

- For D_3, I_{peak} and $\overline{i}_{\mathrm{D}_2}$ depend on the magnetizing inductance L_{m}, so we can't know them.

  The reverse voltage can be specified: we know that it occurs during T_{ON}, so:

$$V_{\mathrm{reverse}} = V_{\mathrm{IN}} + \frac{N_{\mathrm{T}}}{N_{\mathrm{P}}}V_{\mathrm{IN}}$$

- For the switch, we need something different: peak current, minimum current, RMS current, average current, switch reverse voltage, $r_{\mathrm{DS,ON}}$.

  About the maximum current (the peak current), we can use again the transformer equations, and find:

$$I_{\max} = I_{\mathrm{L,max}} \frac{N_{\mathrm{S}}}{N_{\mathrm{P}}}$$

(we have to change numerator and denominator because we are talking about currents). Actually, there is also an extra term:

$$I_{\max} = I_{\mathrm{L,max}} \frac{N_{\mathrm{S}}}{N_{\mathrm{P}}} + i_{\mathrm{m,max}}$$

This is a more complete equation: we missed the magnetizing current.

For the minimum current, we have:

$$I_{\min} = I_{\mathrm{L,min}} - \frac{N_{\mathrm{S}}}{N_{\mathrm{P}}}$$

here we don't have any magnetizing current term, because that term is gone into the tiny-flyback, which cares about it.

About the voltage of the switch, we have:

$$V_{\mathrm{SW}} = V_{\mathrm{IN}} + V_{\mathrm{P}}$$

where V_{P} is the *reflected voltage* respect to the flyback part. So:

$$= V_{\mathrm{IN}} + V_{\mathrm{IN}} \frac{N_{\mathrm{P}}}{N_{\mathrm{T}}} + V_{\mathrm{spike}}$$

we have again this V_{spike} term, which is from 20 % to 30 % of the $V_{\mathrm{IN,max}}$. This is the side effect we mentioned: stress is quite high, and if we increase the primary to tertiary turn ratio, we increase the stress. Our switch will be very stressed. About $r_{\mathrm{DS,ON}}$, we have

$$r_{\mathrm{DS,on}} = \frac{V_{\mathrm{SW,max}}}{I_{\max}}$$

- About C_0, we have the same situation as buck converter.
- About R_{S}, we have the same situation of all times:

$$R_{\mathrm{S}} = \frac{1\ \mathrm{V}}{I_{\mathrm{SW,max}}}$$

- About C_{in}, we must specify at least two quantities: the working voltage, and the RMS current. Working voltage is trivial: just $V_{\text{IN,max}}$; about RMS current, we have something different:

$$I_{C_{\text{in}},\text{RMS}} = I_0 \frac{N_{\text{S}}}{N_{\text{P}}} \sqrt{D - D^2}$$

  the worst value for the root square is 1/2; so:

$$= \frac{1}{2} I_0 \frac{N_{\text{S}}}{N_{\text{P}}}$$

Generally, we set $D_{\text{max}} = 0.5$; this can be set with some circuit, which permits to *blank* over this time. The actual steady state must be something less, because, if the very maximum duty cycle equals 0.5, with $N_{\text{P}} = N_{\text{T}}$, we must have some margin. This margin is not due to tolerances or similar things, but for another reason: it may happens that the load current i_{load} become higher, if load changes; when we increase, due to a load change, the output current, inductor can not provide it, because an inductor can not provide spike currents (current is the inductor's state variable); the only device which can provide the extra current is the output capacitor, which will be discharged, until it loses too much charge, so some voltage, and capacitor voltage equals output voltage. The controller sees that output voltage goes down, and tries to increase the duty cycle, but it is useless: the inductor current must increase in a continuous, smooth way. Controller keeps for asking for more current and so, when L has a good current, and we increase load (asking for less current), inductance has a too high current even if capacitor is charged, and controller saturates.

The maximum D we want in steady state is less than the maximum: if we have some extra-power margin, we have some more *change speed*, so we can increase some kind of acceleration. In order to have a short load-up time, we can use, for example:

$$D_{\text{max,steady-state}} \sim 0.4$$

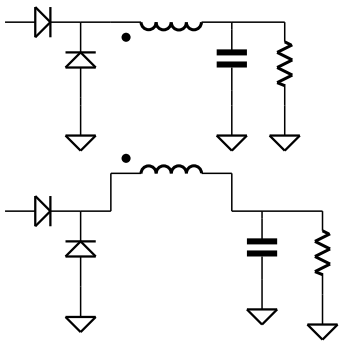
This is like putting the gear off.

Final observations

This converter may give more power respect to the previous ones: it can handle 100 W to 200 W (usually, not more!). This means that it can handle

more power respect to the flyback converter, but it is also much more expensive: it requires two power diodes, and two magnetics: we have an inductor (the buck's one), and a transformer (with the three windings): this is very big, and very expensive.

If we want to get more outputs we need to add another inductor and other two power diodes: this is very expensive, and hard to control: all the windings must be controlled to work in CCM, so we have to guarantee a minimum load in both of them. A better idea may be this one:



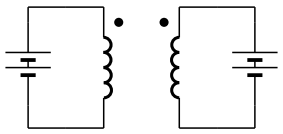
We can wind the two inductors on a single magnetic core, using as condition:

$$\frac{N_{S1}}{N_{S2}} = \frac{V_{01}}{V_{02}}$$

This allows us to have just two magnetics: more complicated than a flyback, but not so worse that the standard forward converter. There is another advantage: we have a single flux for both the new windings, and flux does not drive in DCM.

We have also a better load regulation: the outputs are connected together, because if we change the load on one of the secondary windings, we change the current, and this is sensed by the transformer: we can just connect the feedback to one of the secondary windings, and it will regulate all the windings.

Another advantage: now leakage inductance are **needed**: if we connect two voltage sources through coupled inductors, we have something like this:



Now: this works just if:

$$\frac{V_1}{V_2} = \frac{N_1}{N_2}$$

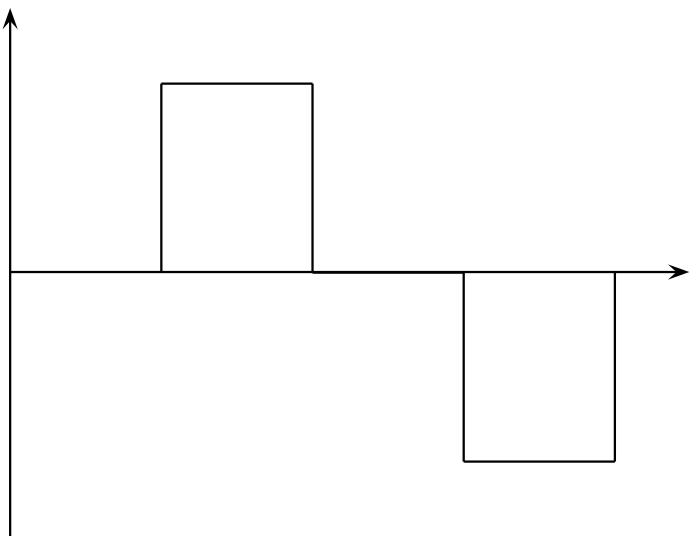
If this is not true, we obtain some kind of short-circuit, in which we have a high current: we can't add two voltage sources in parallel! Leakage inductance so is good, in order to limit this short-circuit circulating current, which is very high. This structure/idea is used for all buck-derived converters.

3.3 Full-bridge converters

Are we happy of the previous converter? Absolutely not! The first transformer is used for just 40% of the time, and for the remaining time we are just discharging the magnetic flux. This means that our converter is used for a very short time.

Our purpose is to exploit this transformer, without driving it into saturation; an idea may be to connect for a time the primary winding to a positive voltage respect to ground, and for another time (which must **equal** the previous one, if voltages are equals) to the same voltage, but negative respect to ground. This allows us to have $\overline{v} = 0$, and to deliver power to the output for more time, increasing the using time of the converter. If we are able to do something like this, we can transfer energy during both charge and discharge phases.

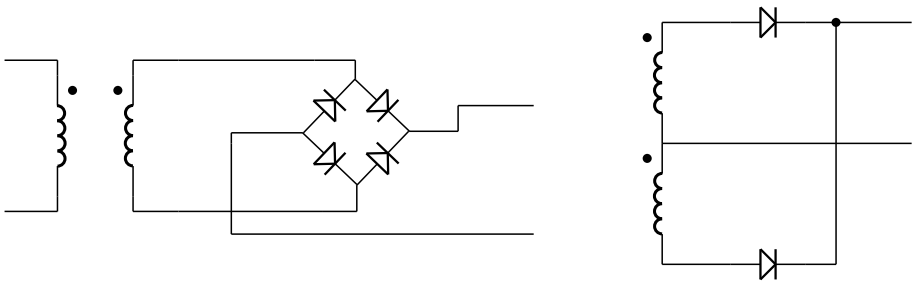
The voltage on the primary (so also on the secondary) winding will be a square wave like this:



This waveform has zero average; this is good from the magnetics point of view, but not good from the output point of view: at the output in fact we need a DC, and we can not obtain it from this waveform. This means that we have to rectify it (let's remark that now we don't know how to realize it, but we will study it later).

In order to rectify this waveform, there are two main solutions:

- using a Grätz bridge (also known as full-rectifier bridge);
- using a center tap transformer.



Let's study the differences between the two rectification techniques.

- The left solution has four diodes, but just one secondary winding; the right one has less diodes, but a more complicated transformer.
- Average current stresses are the same: the i_0 current comes from a node which connects two sides of the circuit in both cases. For a node we can use the KCL, so we have, on each diode:

$$\bar{i}_{\mathrm{D}} = \frac{1}{2}\bar{i}_0$$

- Reverse voltages are different: with Grätz bridge we just have the voltage on the secondary winding:

$$V_{\mathrm{reverse,Grätz}} = V_{\mathrm{secondary}}$$

in the center-tap solution, we have that, if a diode is closed, on it we have twice the secondary winding, because when diode is open, we have on it the two secondary windings voltages:

$$V_{\mathrm{reverse,center-tap}} = 2V_{\mathrm{secondary}}$$

- Also output voltages are different in the two cases: what change are the voltage drops between output and secondary winding? Well, in center tap, we simply have:

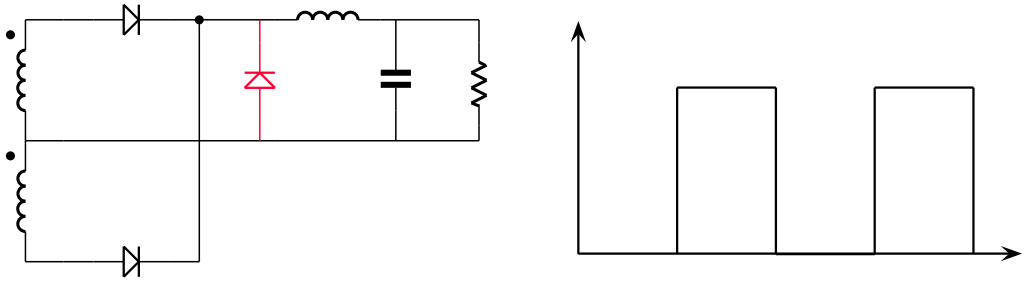
$$V_0 = V_{\text{secondary}} - V_{\text{D}}$$

  We have a voltage drop equal to one diode voltage drop.

  In full-bridge, we have to pass through two diodes, so the voltage drop will be the double of the previous one.

If we are designing a high output voltage converter (50 V up) full-bridge converter is the better choice, because we waste a few volts, but we also have less stress on each diode; on the other side, if we have a low output voltage converter (from 50 V down), this is bad: output diodes are wasting a lot of power, so center-tap solution is the better one.

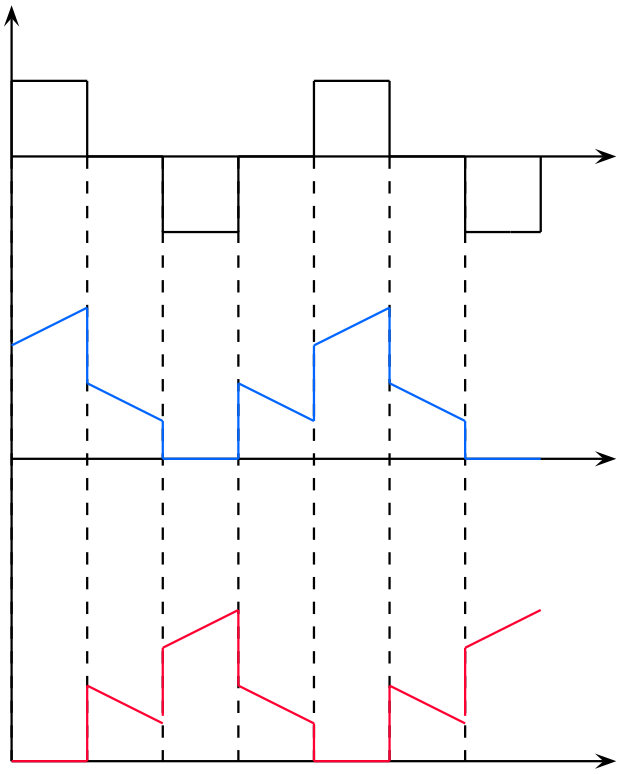
The converter can be completed by inserting the output low-pass filter:



Do we need the free-wheeling diode? Well, we know that the waveform is the previous one, so voltage does not go under zero: this means that this diode is never directly biased, and current just goes through the two diodes. Current, during the T_{OFF} time, will go from the D_1 and D_2 diodes.

When primary winding is on an open circuit (so when the switch is open), how much current goes through D_1 and D_2 ? Well, we have a transformer, and we know that current on each winding depends on the turn ratio of the windings: this means that the current through those diodes depends on the turn ratio of this particular transformer: during this T_{OFF} phase the only windings working in the transformer are the two secondary windings. The two windings, in order to have the same voltage transformation (we are just rectifying, not changing the voltage levels), have the same number of turns, so we have the same voltage and the same current on the two secondary windings.

If we plot the voltage on the secondary windings, and the currents on them, we obtain something like this:



Let's describe this graph: when we have the positive pulse, so during the first T_{ON}, we have that the i_{D1} is positive and increases with a slope like

$$\frac{V_{\mathrm{IN}} - V_0}{L}$$

and i_{D2} is zero. During T_{OFF}, there is something different: both D_1 and D_2 start conducting, with half of the inductor's current; next cycle, when we have the second T_{ON}, the situation reverses: we have $i_{\mathrm{D1}} = 0$, and i_{D2} equal to the inductor current; second T_{OFF} equals the first one. These strange waveforms are the one which we can observe on a scope.

Let's think about what we obtained: supposing that we can realize this ideas, we have to describe the behaviour of this converter, up to the secondary winding, with four steps:

- during the first T_{ON} time, we connect to the primary winding a positive input voltage;
- during the first T_{OFF} time, we keep the primary winding open;
- during the second T_{ON} time, we connect to the primary winding a negative input voltage;

- during the second T_{OFF}, we keep again the primary winding open.

Let's remark that $T_{\mathrm{ON},1} = T_{\mathrm{ON},2}$, and that $T_{\mathrm{OFF},1} = T_{\mathrm{OFF},2}$; this means that, from the primary (and secondary) winding point of view, we have a duty cycle D which must be less or equal to 0.5 : D is the normalized time in which voltage is non-zero, in the square wave; this means that this D must be defined as:

$$D \triangleq \frac{2T_{\mathrm{ON}}}{T_{\mathrm{SW}}}$$

If we have $D > 0.5$, it means that we have (due to the fact that the two T_{ON} are the same) both positive and negative voltages at the same time, and this is absurd!

This D was the duty cycle *seen* from the transformer; after the transformer, we have the buck converter, which is fed by the output of the rectifier; when we rectify this waveform, we obtain a waveform with a period equal to half of the previous period, so with the double of the frequency respect to the previous one (in fact, before of the rectification we had a positive and a negative peak, now we have just positive peaks, so the periodicity changes); now, so, we obtain that:

$$T_{\mathrm{SW,buck}} = \frac{1}{2} T_{\mathrm{SW}}$$

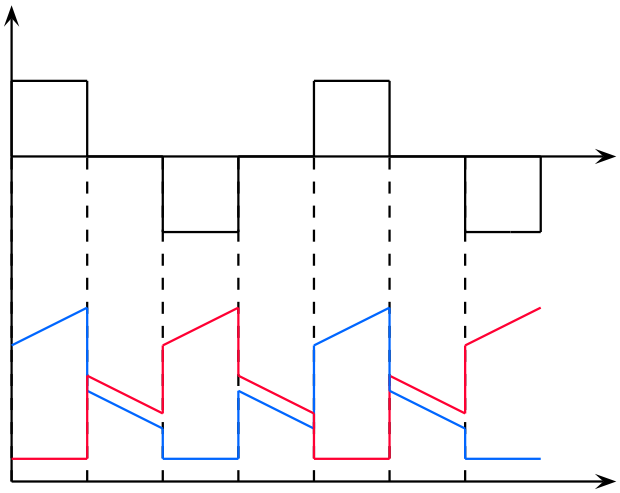
so, considering again the definition of D:

$$D_{\mathrm{buck}} = \frac{2T_{\mathrm{ON}}}{T_{\mathrm{SW,buck}}} = \frac{2T_{\mathrm{ON}}}{\frac{1}{2}T_{\mathrm{SW}}} = 2D$$

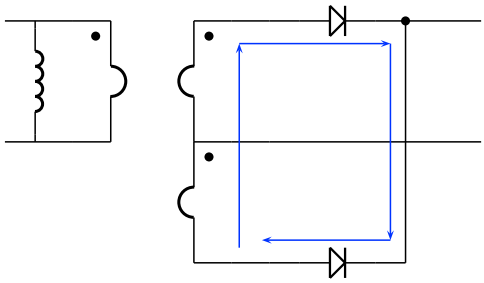
now, the maximum duty cycle is:

$$D_{\mathrm{buck,max}} = 2D_{\mathrm{max}} = 1$$

In our analysis we didn't care about magnetizing current: L, in our magnetic transformer, is not infinite, so it will store some energy as magnetic flux, and it will have some current on it: we have an i_{m}. This i_{m} will unbalance the two descending currents on the two diodes, so the actual waveform will be something like this:



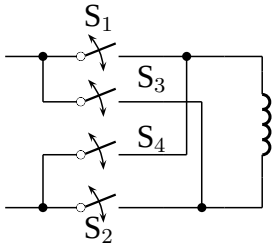
Another remark: in this circuit, we have that, even if we don't have any voltage feeding it, during T_{OFF} there is some current into the secondary winding. Why?



Well, this question is stupid! This question presupposes that we are applying some kind of superposition principle, but this circuit has diodes, so it is a **non-linear circuit**! We have the inductor current, and some non-linear elements, so even without biasing there is some current, due to the non-linearities of this system.

3.3.1 Realization of the input stage

How to solve the problem of the input stage? How to realize the bi-polar voltages? Well, the idea is to use two couples of switches, in this way:



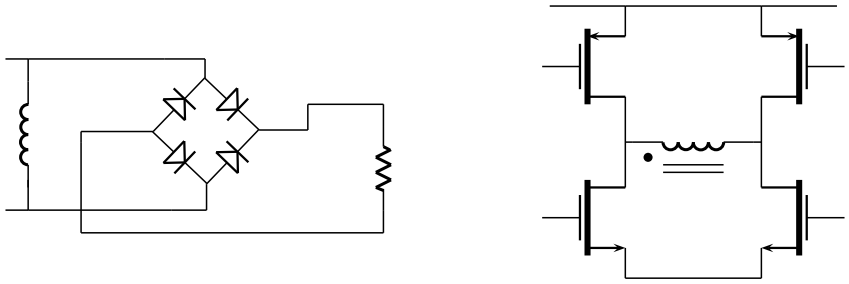
When we close S_1 and S_2, we have, as voltage:

$$V_{\mathrm{P}} = V_{\mathrm{IN}} - 2V_{\mathrm{SW}}$$

When we open S_1 and S_2, and close S_3 and S_4, we have:

$$V_{\mathrm{P}} = -V_{\mathrm{IN}} + 2V_{\mathrm{SW}}$$

Actually, this can be simply realized with a Grätz bridge, or with an H switch:

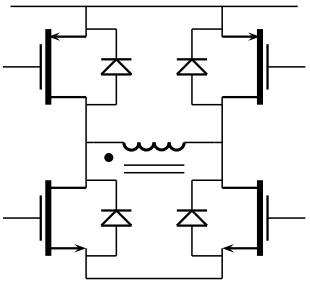


Let's remember that the maximum D, for each one of these switches, is 50%, in order to obtain zero DC voltage.

Our C_{in} capacitor experiences, each time we close the switch, a current pulse; which is the frequency for these pulses? Well, it is the **buck** f_{SW} (so $f_{\mathrm{SW,buck}}$): one time we open, one time we close, so we have all those pulses running on them.

A disadvantage of this structure is the fact that there are many switches; there are many integrated circuits which can realize those functions.

This structure has also many advantages: we are using our transformer for a long time (80% of the switching period). If we realize the H-bridge with MOS transistors, we have another advantage:



For free our transistors have a body diode, so the maximum voltage that the switches can experience can not be more positive than the V_{IN} voltage: those diodes act as clamping diodes, so they limit the maximum voltage drop

to V_{IN}. This means that, respect to forward, we don't have spikes (because they are clamped), and so much less stress.

This topology is very good for high input voltage and power converters, because it doesn't stress too much the various components. If we have low input voltages, from the other hand, we can not use it, because we have that:

$$V_{\text{P}} = V_{\text{IN}} - 2V_{\text{SW}}$$

in the primary winding we have many losses: this is not good. From 200 V up it can be a very good converter.

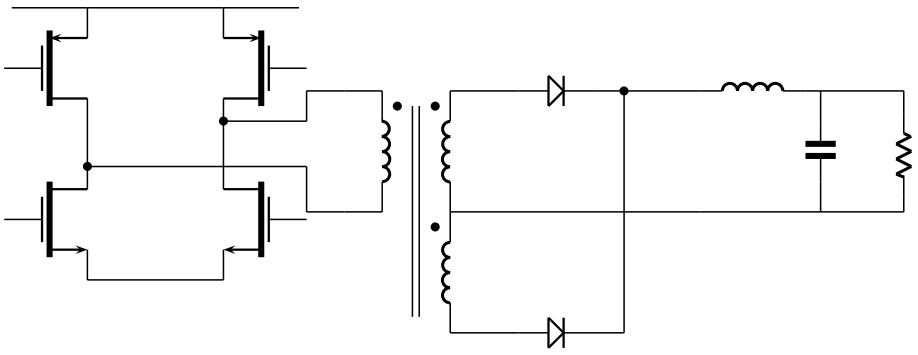
What about the other stress components? Well, we have $\overline{i}_{\text{SW}}$ and $\overline{i}_{\text{IN}}$. About $\overline{i}_{\text{IN}}$, (1) is a node, so we can use, for averages, the KCL; we have that:

$$\overline{i}_{\text{SW}} = \frac{1}{2}\overline{i}_{\text{IN}}$$

each transistor will experience half of the input current.

This topology is named full-bridge, and it is good for high powers, because it reduces stresses. It can be used from 500 W up. If we design large transistors and other components, this topology can work also with 1 MW.

Let's study the design equations:



This is quite similar, from the formulas point of view, to the forward converter:

$$V_0 = (V_{\text{IN}} - 2V_{\text{SW}})\frac{N_{\text{S}}}{N_{\text{P}}}D_{\text{buck}} - V_{\text{D}}$$

As degree of freedom, we can choose $D_{\text{buck,max}}$; it can be $0.8 \div 0.9$ (we have to take account of the *acceleration issue*). About the inductance:

$$L > \frac{(1 - D_{\text{buck,min}})R_{\text{max}}}{2f_{\text{SW,buck}}}$$

This is a high power topology, so it requires low switching frequencies (about 50 kHz).

In order to perform the design, we have to estimate $D_{\min}$; there is an approximated formula, which gives:

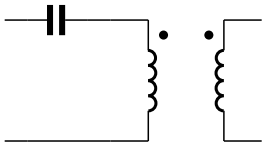
$$D_{\min} = D_{\max}\frac{V_{\text{IN,min}}}{V_{\text{IN,max}}}$$

A complicated parameter to evaluate (the only one which changes from the previous cases) is the RMS current, of the strange waveform of the diodes; we can just perform some flat-top approximations and get rid of them.

Just one more final note: we can **not** guarantee that:

$$T_{\text{ON,S}_{1,2}} = T_{\text{ON,S}_{3,4}}$$

this, because of tolerances. This means that we may have DC components. How to erase them? Well, simply by putting a capacitor in series to the primary winding:



We want that this capacitor blocks DC and allows current to go forward and backward; when current goes through it, it charges/discharges, so, by inverting its equation, we obtain:

$$\Delta v_{\text{C}} = \frac{1}{C}\int_0^{T_{\text{ON}}} i_{\text{P}}\text{d}t$$

This derives from the fact that:

$$\Delta v_{\text{C}} = \frac{\Delta Q}{C}$$

Usually we design Δv_{C} in order to have:

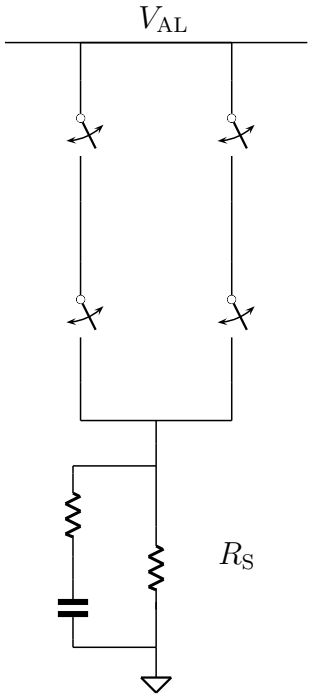
$$\Delta v_{\text{C}} \ll V_{\text{IN,min}}$$

In order to evaluate the integral, so the amount of charge ΔQ, we may calculate i_{L}; this may be done by considering the output voltage, reflected on the primary winding:

$$i_{\text{P}} = I_0\frac{N_{\text{S}}}{N_{\text{P}}}$$

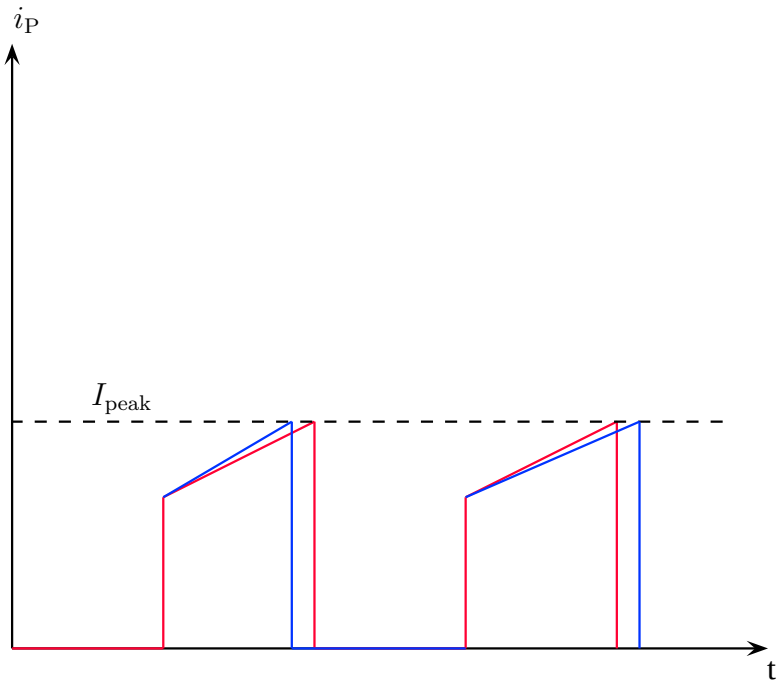
Let's remark that this capacitor does not add any loss: one time we increase voltage on it with a polarity, one time we increase it with the other polarity, so in average we have zero extra voltage due to this capacitor. Let's remark that our capacitor can resonate with the inductance, introducing some kind of oscillation; this is not too bad, so we can ignore this effect and do the design.

This capacitor must be used if we want to control in **voltage mode**. What about current mode? Well, we need to measure current, instead of voltage, and we can do it on the primary side, in order to protect our switches from the transformer saturation. We have to measure current for both the T_{ON} times; so putting it in series of the transformer may be a bad idea: voltage swings up and down, and this is a common mode voltage; current goes in opposite directions in the two cycles, so we have to use another idea. The best idea is this one:



We put the two switch couples together and put R_{S} between them and ground. If we want to add the current mode control, we can also introduce the low-pass filter.

Our pulses will have a waveform like this one:



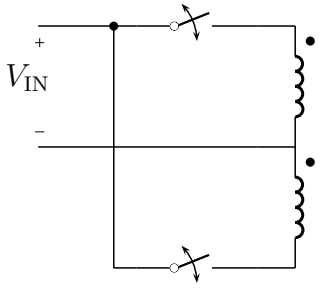
This is the behaviour of $V_{R_{\mathrm{S}}}$: we have pulses with the same polarity. Let's remark that we have also another current, on the primary winding: the **magnetizing** current, which may introduce some problems: i_{m} can be a little higher or lower respect to the ideal, to the expected one, and this is added to the current reflected from the secondary winding; this can change the voltage drops on the various points of the circuit, so the measured quantities. Current mode control senses the **peak** value, so an extra unbalance current introduces some changes respect to the ideal case: one pulse will be narrower the following one wider, and so on. The fact that current mode stops this, permits to keep our global system balanced.

A remark: we are not using any C_{p} capacitor, so any capacitor which must stop DC; may we use it? Well, if we do it, we obtain a no-working system: current mode maintains constant the peak value, but not the area of the pulses, so the behaviour of the capacitor is conditioned by the behaviour of the current mode controller.

Final question: do we need a compensation ramp, for current mode control? Well, the duty cycle we have to consider is the **buck converter** one, because it could be unstable! And it is the double of the switch duty cycle: we definitely need a compensation ramp.

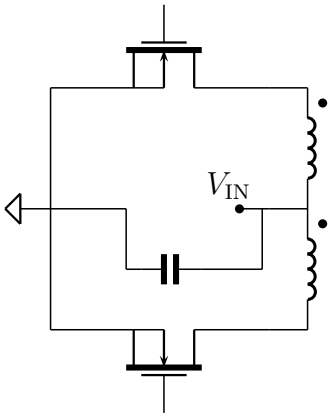
3.4 Push-pull converter

Let's consider something different respect to the full-bridge configuration: what happens if we use MOS switches instead of diodes, with the center-tap configuration used as **driving** configuration? Well, we obtain something like this:



we have a center-tap primary winding, two switches instead of the two diodes, we put them together and connect the center of the center tap to ground, and the two switches to V_{IN}.

Well, the idea is good, but it has a problem: now our switches are connected to a positive voltage, but this means that they are **high-side** transistors, and we don't like them! Let's consider this circuit:



This is the **push-pull** topology: it derives from a center tap rectifier, and it has the same properties:

$$\overline{i}_{\text{SW}} = \frac{1}{2}\overline{i}_{\text{IN}}$$

this, because for one half of the cycle current goes through S_1, for the other half through S_2. This means that we reduce current stresses on the switches.

About the reverse voltage, we have that, when one transistor is *closed*, all voltage goes to the *open* one:

$$V_{\mathrm{SW,reverse}} = 2V_{\mathrm{IN}}$$

this is bad: we have twice the input voltage, on a single transistor: this is bad under the voltage stresses point of view.

The third parameter was the voltage drop between input and primary winding: now we have, for each half-cycle, in series to V_{IN}, just one switch.

This topology is good for low input voltages, due to the high stresses, but may be used for high powers, thanks to the low input current stresses; it can work from $100 \div 200$ W up.

What about the control for this topology? Do we prefer to control it in voltage or in current mode? Well, we have to remember the flux-runaway problem: each time we charge and discharge a transformer, we risk to saturate it, and damage the problem. Can we introduce the C_{p} capacitor before the primary winding? Absolutely no! It can not be introduced there, because it goes in series to the DC voltage: we have no place for C_{p}, so we have to use current mode.

Actually, sometimes voltage mode works: this because if we have flux runaway, we may have higher average voltage in one side respect to the other side, so in some cases the parasitic resistances of the transistors may dissipate the magnetizing current and prevent saturation. With bipolar transistor is even worse, because if we have two transistors with different currents, we heat up one transistor more than the other. Bipolar transistors have long switching time, so we need a long time to put the switch off, we apply a longer pulse on them, and it may be damaged or destroyed.

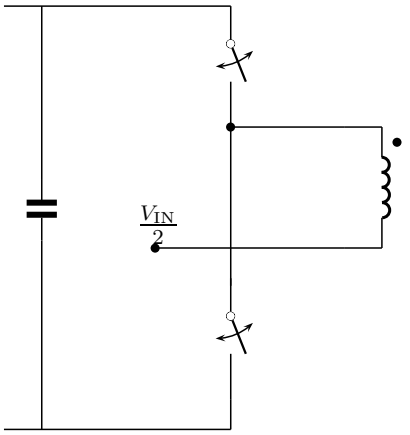
Supposing that we are using control mode, we have that output voltage equals:

$$V_0 = \left(V_{\mathrm{IN}} - V_{\mathrm{SW}} - V_{R_{\mathrm{S}}}\right) \frac{N_{\mathrm{S}}}{N_{\mathrm{P}}} D_{\mathrm{buck}} - V_{\mathrm{D}}$$

Under some points of view, this topology is better than the full-bridge one: now we have one switch voltage drop instead of two of them, because now we have just one switch between the input voltage and the primary winding. The inductance must be designed exactly as in a full-bridge power converter. The limitation of this topology is the fact that we **must** use current mode controls.

3.5 Half-bridge converter

Let's consider this circuit:



Let's suppose that, in some way, we are able to introduce half of the input voltage (it will be very easy); when we close S_1, we have that:

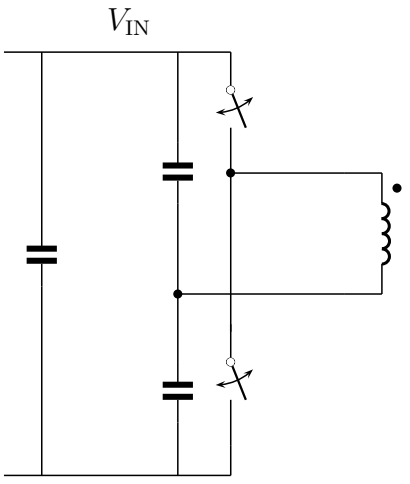
$$V_{\text{P}} = \frac{V_{\text{IN}}}{2}$$

and, when we close S_2 and open S_1, we have:

$$V_{\text{P}} = -\frac{V_{\text{IN}}}{2}$$

This permits to drive the primary winding with positive and negative voltages, so to avoid saturation.

In order to realize this, we can use a circuit like this one:



a capacitive voltage divider: we can not use inductors, which are short circuits respect to DC (and more expensive), and we prefer to avoid resistances (which introduce losses, reducing the efficiency η), so capacitors are our best choice.

What about the final parameters for this topology? Well, we can see that the maximum reverse voltage across each switch equals the input voltage:

$$V_{\text{SW,reverse}} = V_{\text{IN}}$$

About the average current respect to the input one:

$$\overline{i}_{\text{SW}} = \overline{i}_{\text{IN}}$$

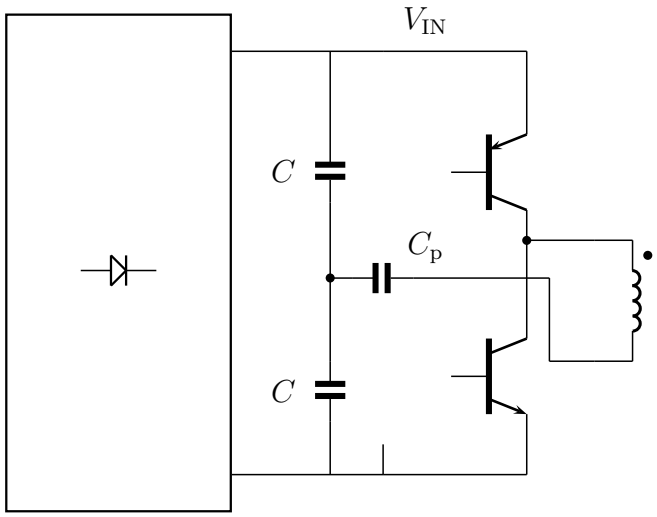
in fact, when a switch is closed (and the other one is open), all the current flows through it; capacitors obviously have no average current! And, obviously, we have just one switch between input voltage (which is halved) and output voltage.

This circuit is perfect for high input voltages, and relatively high current stresses (it depends on the input current, actually, so it is worse respect to the push-pull): it can handle medium power levels (quite high powers, but less respect to full-bridge); this, due to the capacitors: about $500 \div 700$ W are good. Usually, we put a PFC in front of it, and then it.

In this circuit, we can use voltage mode thanks to the capacitive divider: adding a capacitor can be easily done, as we will show in a moment. The output voltage equation for this circuit is:

$$V_0 = \left(\frac{V_{\text{IN}}}{2} - V_{\text{SW}} \right) \frac{N_{\text{S}}}{N_{\text{P}}} D_{\text{buck}} - V_{\text{D}}$$

A typical use of this converter is in PC (Personal Computers), desktops; the schematic we usually find is this one:



There is also the C_{p}, between the capacitive divider and the inductor. Usually, we introduce electrolytic capacitors, for 200 V (our main voltage), of something similar to 200 μF. These two capacitors cost less than one single capacitor which handles 400 V, so we can rectify our main voltage and obtain our converter. The C_{p} capacitor is very important, because the two main capacitors have a too high capacitance, and we risk to saturate the transformer before charging them.